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FMC ADC 1G 8b 2cha Design Manual

Sundance FM582

Abstract

This design manual describes the proposed design of the high speed 1G sample per second 2 channel FMC ADC board. The design is based on the design study published on 20th February 2019, and the requirements published by CERN.

The architecture uses the FPGA on the FMC carrier, with parallel communication over the FMC LPC connector. This supports 2 data acquisition channels. The different sampling rate options supported are 2 channels at up to 1GS/s each, or 2GS/s on one channel only. The design also provides an external trigger input and output, and an external clock input and output.

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Revision History

Issue	Changes Made	Date	Initials
1	First draft	31JAN20	SEC
2	Add 2V5 VADJ description. Change synthesiser to LTC6951 with 25MHz reference VCXO. Added FMC signal mapping. Revised all entries post design.	10NOV20	SEC
3	Added photos	21.07.21	FC

Table of Contents

Table of Figures

1 Foreword

This design manual describes all aspects of the design of the FMC ADC 1G 8bit 2 channel board. It describes the architecture first, then goes on to describe each sub section in detail.

The design study is based on the requirements in the CERN specification below, which are copied directly from this web site:

https://www.ohwr.org/projects/fmc-adc-1g8b2cha/wiki

Parameter	Value
PCB format	VITA 57.1 FMC LPC
Connectors	SMA
Sampling Rate	1 GSPS (preferably 2GSPS)
Input Signal Type	single-ended
Resolution	8 bits
Number of Channels	2 (preferably 4)
Bandwidth (-3dB)	50Ω: DC to 400MHz (or better)
	1MΩ: DC to 300MHz (or better)
	AC (8 Hz LF limit, after 50 Ω termination)
Input Signal Coupling and Termination	DC-50Ω
	DC-1MΩ
Input Signal Range	+/- 50mV
	+/- 250mV
	+/- 500mV
	+/- 2.5V
	+/- 5V
Max Input Signal Amplitude	+/- 10V
SNR	> 40dB full bandwidth over all input ranges
ENOB	> 6.5 full bandwidth over all input ranges
Offset Adjustment Range	+/- 5V

Offset Adjustment Resolution	16 bits
Offset Adjustment Accuracy	< 1%
Additional I/O	External TTL trigger in/out (bidirectional) External 10MHz clock input
Self-calibration	Automatic zeroing of offset and gain
ADC interface	serial/parallel LVDS
Temperature sensor	via one-wire ds182x
FMC EEPROM	24C02, as per VITA 57.1
Power Consumption	< 7W

Notes:

The following features should be controllable by software:

- Input signal range, coupling, termination and offset adjustment
- Self-calibration
- Sampling clock selection
- Direction of external trigger in/out
- ADC configuration and status

The offset adjustment must not clip the signal at the highest range (+/- 5V). That is why the "max input signal amplitude" has been specified as 10V, even though the selection of signal ranges only goes up to 5V. This way, a +10V pulse with -5V offset could still be digitised without clipping.

The sampling clock should be derived from a voltage-controllable 125MHz clock source, controlled via an SPI DAC.

A copy of the 125MHz clock source should be available on the FMC connector pins.

Additional requirements not published above:

1. The VITA standard used for the design is “AV57DOT1-2019.pdf” dated: 1st February 2019.
2. Over Voltage protection +/-100V at DC-1M Ohms. This is taken to mean continuous protection from a constant DC +/-100V, not just a transient.
3. Over dissipation protection for the 50 Ohm termination.
4. Separation of the SPI control signals is required to allow continuous control of each of the following: The 125MHz VCXO (to implement a digital phase locked loop), ADC1, ADC2. Other SPI controls can be combined.
5. Industry expectation 1: The 1M Ohm input will have a capacitance between 10pF and 20pF.
6. Industry expectation 2: The 50 Ohm input will have a VSWR of less than 1.3 at 500MHz and less than 1.5 at 1GHz.

2 Input Architecture

The signal input specification represents a very challenging design requirement. The maximum signal amplitude is specified as +/-10V, made up of a DC offset of +/-5V plus an AC signal of +/-5V.

A programmable offset adjustment is required with a range of +/-5V, which is subtracted from the incoming signal. This allows the operator to completely remove the incoming DC offset, so that the AC signal has a DC offset of 0V.

An AC coupling (high pass) switch is specified, with low frequency -3dB of 8Hz.

Five input gain ranges are specified giving a full scale of between +/-5V and +/-50mV.

Two different input impedance are specified:

50 Ohms with -3dB bandwidth of at least 400MHz. Note that 10V across 50 Ohms is 2 Watts.

1M Ohms with -3dB bandwidth of at least 300MHz

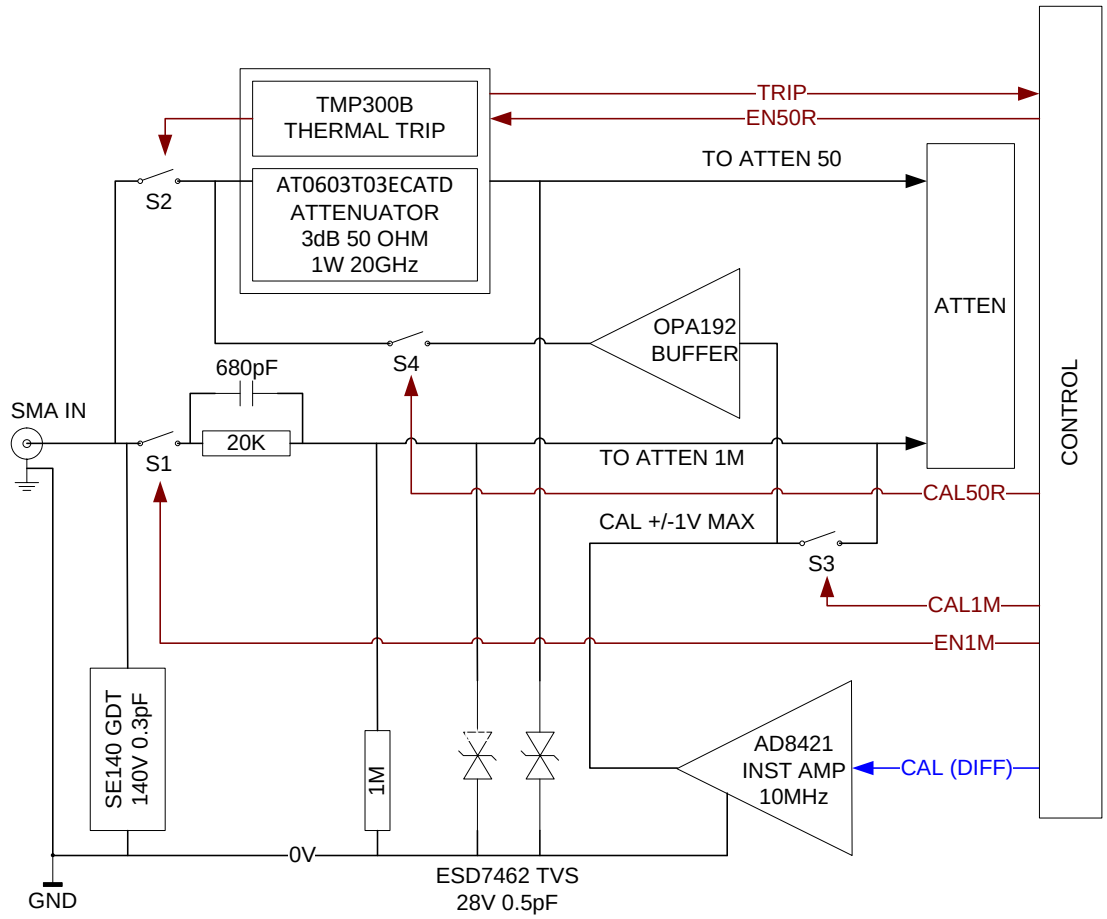
The input must be able to survive a transient or continuous input of +/-100V at ALL times. There is no restriction on disconnecting from the input signal under overload conditions, as a 2 Watt 50 Ohm load cannot be permitted to stand a dissipation of up to 200 Watts. An overload disconnect must be reported as an error condition.

Note that this requirement means that a high voltage safety warning MUST be clearly displayed.

Inputs in excess of +/-100V, such as ESD discharge, which could damage input structures, should be discharged to chassis.

The following table is provided for information about sine wave signal levels:

Volts pp	**Volts RMS**	**dBm (50 Ohms)**
+/-28.28	10.0	33
+/-20.0	7.071	30
+/-10.0	3.535	24
+/-5.0	1.768	18



Notes:
S1 & S2 are Standex Meder CRF05-1A reed relay 170V 0.2R 0.5pF 7GHz
S3 & S4 are Panasonic AQY221N2T photomos relays 40V 12.5R 1.5pF
1M Ohm input rated to +/-100V continuous
50 Ohm input rated to +/-10V continuous (2 Watts)
Signal + Offset +/-10V Max
Signal Full Scale +/-5V to +/-50mV
VSWR < 1.3 at 500MHz 50R
Thermal TRIP disables S2

Figure 1: Input Architecture

2.1 Input switching and protection

The inputs are protected from voltages greater than +/-100V, by SE140 Gas Discharge Tubes (GDT) made by Littlefuse. The GDT is commonly used in lightning protection systems, and is the only device available which can pass a surge current of 500 Amps, with a normal capacitance of less than 0.5pF.

These are rated as follows:

1. DC breakdown 98V min, 140V typ, 182V max
2. Impulse breakdown 800V at 100V/us
3. Capacitance 0.5pF maximum
4. Current rating >500A

https://www.littelfuse.com/products/gas-discharge-tubes/squared-gdt/se.aspx

A key architectural decision is how to implement the input impedance switching between 1M Ohm and 50 Ohm. The industry expectations 1 and 2 listed above are:

1. Industry expectation 1: The 1M Ohm input will have a capacitance between 10pF and 20pF.
2. Industry expectation 2: The 50 Ohm input will have a VSWR of less than 1.3 at 500MHz and less than 1.5 at 1GHz.

These cannot both be met by switching a 50 Ohm terminating resistance across a 1M Ohm input which is shunted by 10pF. At 500MHz a 1.75pF capacitor across a 50 Ohm terminator gives a VSWR of 1.31, and a 10pF capacitor gives a VSWR of 3.14 at 1GHz. These facts force us to implement separate input paths for the 50 and 1M Ohm inputs.

The requirement to withstand +/-100V without damage, and to switch between 50 and 1M Ohms inputs, forces us to use mechanical relays specified for more than 100V, because there are no low capacitance electronic switches that have this voltage rating. S1 switches the input to the 1M Ohm path, and S2 switches the input to the 50 Ohm path. These switches are CRF05-1A reed relays made by Standex Meder, and rated as follows:

1. Switching Voltage 170V maximum
2. Contact resistance 200 mOhm maximum
3. Capacitance when open 0.5pF maximum
4. Switching current 0.5A maximum

https://standexelectronics.com/products/crf-series-reed-relay/

These relays are only available as Single Pole Single Throw (SPST), so we have to use one for each input path.

2.2 50 Ohm Input path

This input has a 50 Ohm path for DC at all times. The AC high pass switch is implemented after the 50 Ohm termination. To implement a switched 8Hz high pass response before the 50 Ohm termination requires a 398uF capacitor, which is not practical in this environment.

The input is specified to support a maximum voltage swing of +/-10V, made up of an offset of +/-5V plus a signal of +/-5V. A static or slowly changing input of +/-10V can result in the same power dissipation in the 50 Ohm impedance as a 10V RMS signal (+33dBm) which is 2 Watts. There is no low frequency limit to the AC signal specified, so the design must support a continuous input of +/-10V.

The input signal from S2 drives a monolithic 3dB attenuator to reduce the maximum amplitude of the signal from 33dBm to 30dBm. This is done to provide input overload detection, as well as to attenuate the incoming signal, and help to maintain the external VSWR. It also provides some damping in the event the input is connected to an inductive signal source.

An input greater than +/-10V or 33dBm will result in excessive dissipation and overheating in the 3dB attenuator. The temperature of the monolithic 3dB attenuator is monitored with a thermostat. The over temperature trip turns off S2, disconnecting the input. This trip signal is also fed to the control section to generate an interrupt at the FMC interface.

The 3dB attenuator is AT0603T03ECATD made by ATC. With a DC input at +10V the output into 50 Ohms is +7.08V and the attenuator dissipates 1.0W. This is a “PI” filter consisting of a pair of 292.4 Ohm resistors to 0V, connected by a 17.6 Ohm resistor. The package is 0603 and it has 3 terminals with a central ground pad. It is rated to operate at up to +150˚C and up to 20GHz, and to dissipate 1W:

www.atceramics.com/UserFiles/AT_attenuator.pdf

The 3dB attenuator temperature is monitored by a TMP300B thermostat made by TI, which is located in very close proximity to the attenuator. This thermostat has resistor programmable trip point set to 100˚C. The trip disables S2, to disconnect the incoming signal, and is fed to the control section to generate an interrupt on the FMC bus.

https://www.ti.com/lit/gpn/tmp300

The output of the 3dB attenuator is clamped to +/-28V by ultra low capacitance (0.3pF typ) ESD protection diode ESD7462, made by On Semiconductor. This is located after the attenuator, which provides series resistance to dissipate an incoming surge.

https://www.onsemi.com/products/isolation-protection-devices/esd-protection-diodes/esd7462

The output of S2 is also connected to S4, a photomos switch type AQY221N2T by Panasonic, which can switch in a buffered copy of the local CAL signal. It has an off output capacitance of 1.5pF maximum, and an on resistance of 12.5 Ohms. With S2 open and S4 closed, the 50 Ohm input can be calibrated.

The OPA192 buffer dissipation limits the maximum CAL signal to +/-1V. This is because the 50 Ohm input must be driven with +/-20mA to reach +/-1V, and the buffer is supplied from +/-5V. The maximum buffer dissipation is 4V x 20mA = 80mW.

https://www.panasonic-electric-works.com/uk/productfinder-photomos.htm/catalog/PHOTOMOS/PM_RF_VSSOP1_FA_CR10/AQY221N2TY

The series resistance of S4 is 12.5 Ohms maximum, which drops 250mV at 20mA. To correct for this drop, S4 is included in the feedback loop of the OPA192 opamp used as a buffer. A series resistor is used to isolate the OPA192 negative input capacitance from the main 50 Ohm signal path.

https://www.ti.com/lit/gpn/opa192

2.3 1M Ohm input path

The signal from S1 is fed to a parallel 20K resistor and 680pF capacitor, and the output is clamped to +/-28V. This allows the input to be set to +/-100V indefinitely, while the 20K resistor dissipates 259mW, and limits the DC current to 3.6mA.

The output is also connected to a 1M resistor, so that the total external input impedance is 1.02M Ohms. These resistors attenuate the DC signal by a factor of 0.980. The 680pF capacitor forms a potential divider with the 12pF nominal input capacitance, which also divides the AC signal by a similar amount, in order to ensure a flat frequency response. The very small attenuation factor means that the component values are not critical, and the frequency response is not sensitive to component tolerance.

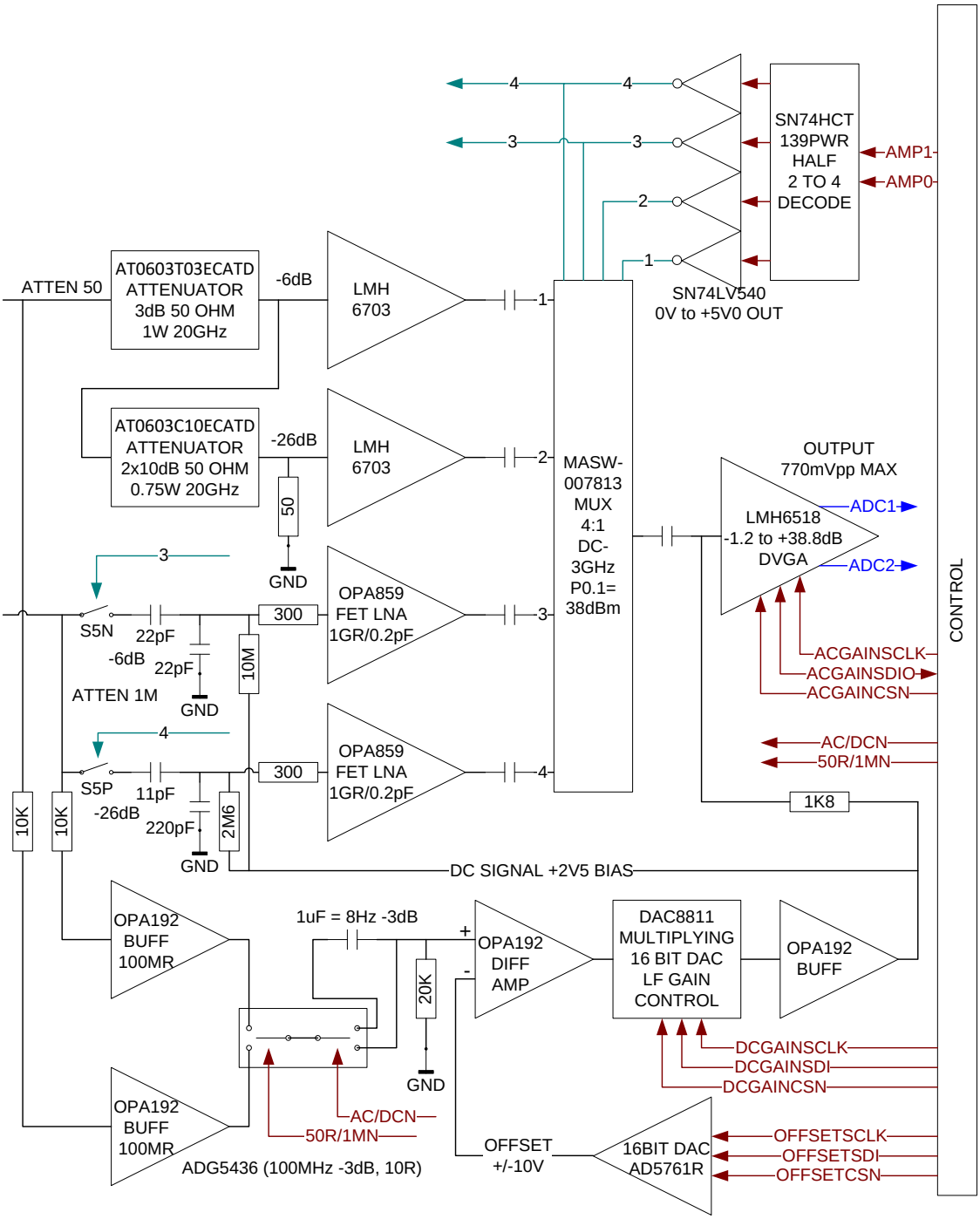
S3 is an AQY221N2T photomos switch, which can connect the local CAL signal to the input. This switch does not create a significant voltage drop because of the high impedances, however it does add 1.5pF to the total input capacitance.

2.4 Local input CAL signal

The CAL signal is converted from differential to single ended by an AD8421 instrumentation amplifier. The AD8421 and the local CAL signal are referenced to the local 0V close to the SMA input connectors. This architecture prevents any voltage drop in the ground plane from affecting the local CAL signal. The differential CAL signal can have a high level of common mode noise which is also rejected by the AD8421. The AD8421 has a bandwidth of 10MHz at -3dB, allowing calibration frequencies up to at least 1MHz without significant distortion. The CAL signal rise time from the AD8421 is estimated at 35ns. The CAL signal should be disabled during normal acquisition to avoid introducing coupled noise into the acquired signal.

https://www.analog.com/en/products/ad8421.html

3 Attenuator Architecture



Notes:
ATTEN 1M input capacitance 12pF +/-0.5pF
S5P & S5N are Panasonic AQY221N2T photomos relays 40V 12.5R 1.5pF
S5P is ON when S5 is true, S5N is ON when S5 is false
OPA192 is implemented as a quad opamp OPA4192

Figure 2: Attenuator Architecture

The attenuator consists of:

1. A 4 way multiplexor
2. 2 separate 50 Ohm attenuation paths
3. 2 separate high impedance input attenuators and buffers
4. A low frequency stage with programmable offset and gain and switched 8Hz high pass filter
5. A differential output amplifier

3.1 50 Ohm attenuator

The 50 Ohm signal from the input stage is fed to a single 3dB attenuator, which combined with the 3dB input attenuator provides a total of 6dB attenuation. This equates to a maximum output of +/-5V, which has a peak to peak level equivalent to an RMS of 1.768V or 18dBm.

This -6dB signal is buffered by an LMH6703 amplifier by Texas Instruments:

https://www.ti.com/lit/gpn/lmh6703

The LMH6703 has the following features:

1. 1800MHz bandwidth at a gain of 1
2. 0.5ns rise/fall time for 2V step
3. 4200V/us slew rate
4. 1M Ohms / 0.8pF non inverting input impedance
5. 2.3nV/sqr(Hz) noise at 1MHz

The input to this buffer is protected with very low capacitance PIN diodes, type BAR63-04W by Infineon:

https://www.infineon.com/dgdl/Infineon-BAR63SERIES_DS-DS-v01_01-EN.pdf?fileId=5546d4625e763904015ec363284f64d0

The buffer output is capacitor coupled to an input of the 4 way multiplexor.

The -6dB signal is also connected to a 10dB attenuator, which in turn is connected to another 10dB attenuator, type AT0603C10ECATD by ATC, to make an overall attenuation of the external input signal by 26dB.

www.atceramics.com/UserFiles/AT_attenuator.pdf

This -26dB signal is buffered by an LMH6703 amplifier by Texas Instruments.

The buffer output is capacitor coupled to an input of the 4 way multiplexor.

Significant attention to detail is required in the pcb layout to achieve a total of 26dB (20 times) attenuation at high frequencies. This equates to a maximum signal output of +/-0.5V, which is terminated by 50 Ohms. This -26dB signal is buffered by another LMH6703 amplifier, and capacitor coupled to an input of the 4 way multiplexor.

3.2 1M Ohm attenuator

The 1M Ohm signal from the input stage is split and fed to 2 photomos switches S5N and S5P, type AQY221N2T by Panasonic. The switches are controlled with the same signals (3 & 4) that control the 4:1 multiplexor. Each photomos switch feeds a high impedance attenuator with an input capacitance of around 11pF.

https://www.panasonic-electric-works.com/uk/productfinder-photomos.htm/catalog/PHOTOMOS/PM_RF_VSSOP1_FA_CR10/AQY221N2TY

Traditional high impedance attenuators consist of a resistive attenuator and matching capacitive attenuator, with the RC time constant of the top and the bottom exactly matched to give a flat frequency response. The level of matching required cannot be obtained without using adjustable capacitance or resistance, because of component tolerances and stray capacitance. This typically involves a mechanical adjustment which must be set during production, adding significant time and cost. The mechanical adjuster is large compared to other modern components. To avoid this issue, only the capacitive attenuator is implemented, with the DC and low frequency signal attenuated separately.

The 6dB attenuator is implemented with a pair of 22pF capacitors in series, giving 11pF load to the input signal. The very high impedance attenuator output is buffered with an OPA859 FET opamp. This new commercial device from TI is the first to have sufficient performance for this role in a monolithic device. Previously this function was implemented with a discrete JFET input amplifier or with a custom device.

https://www.ti.com/lit/gpn/opa859

The OPA859 has the following features:

1. 900MHz gain bandwidth product
2. 0.3ns rise/fall time
3. 1150V/us slew rate
4. 1G Ohms / 0.2pF differential input impedance
5. 3.3nV/sqr(Hz) noise at 1MHz

The slew rate limits the maximum signal amplitude at high frequency. The following equation gives the peak maximum output signal for different frequencies of interest:

Vpk = SR / 2 x pi x freq

MHz	Vpk	Vpp	Vrms
300	0.610	1.22	0.431
400	0.457	0.914	0.323
450	0.406	0.812	0.287
500	0.366	0.732	0.259

The OPA859 drives an LMH6518 which has a maximum differential input of 0.8Vpp, so the OPA859 can be used to drive this input at maximum up to 450MHz, without reaching the slew rate limit.

The noise level is specified at 1MHZ, and below this frequency the noise rises. The output of the OPA859 is capacitor coupled to the multiplexor, which is in turn capacitor coupled to the LMH6518 output amplifier. These capacitor couplings form a high pass filter, which reduces the impact of the rising noise at lower frequencies.

The 26dB attenuator is implemented with an 11pF and 220pF capacitor which form a 20 times divider, with an input capacitance of 10pF. The output is buffered with another OPA859, because it is not possible to switch the inputs to a single OPA859 at such high impedances and frequencies. The 1.5pF off capacitance of a switch looks like a series impedance of just 212 Ohms at 500MHz. So a switch can only be used before the attenuator, where the 1.5pF only adds to the overall attenuator capacitive load.

The OPA859s are powered from +5.0V, and have the following common mode ranges:

1. Input common mode range +0.4V to +3.4V
2. Output common mode range +1.15V max to +3.95V min
3. Combined common mode range as a follower +1.15V to +3.4V
4. With +2.5V input bias, signal range is +2.5V -1.35V, +0.9V

The OPA859 input signal must meet a number of design criteria:

1. Remain within the combined common mode range
2. Provide the OPA859 input bias current of +/-5pA
3. Have a good low frequency response, to guarantee sufficient overlap with the DC path attenuator bandwidth, to avoid phase induced distortion.

The 6dB capacitive attenuator, which feeds the OPA859, consists of a pair of 22pF capacitors in series, so the attenuator output impedance is 44pF. The OPA859 input

impedance is 1G Ohms typical, which means the low frequency response is limited by the OPA859 to:

1 / (2 x pi x 44E-12 x 1E9) = 3.6Hz

To avoid significantly compromising the low frequency response, a very high value bias resistor is required. However resistors above about 50M Ohms are not considered practical because of leakage issues. Simulations show that a resistor of at least 100M Ohms is required.

To solve these issues, the design uses 10M & 2.6M Ohm bias resistors, which are driven by the output of the DC path attenuator. These resistors have almost exactly the same signal at both terminals, over the bandwidth of the DC path attenuator. This makes the resistor behave as if it were a very much higher value, so it does not compromise the OPA859 low frequency bandwidth. It also provides a DC bias of +2.5V, because this is the DC attenuator output bias.

The signal from the DC attenuator is overridden by the signal from the capacitive attenuator, once the capacitive attenuator output impedance falls below that of the bias resistor. This occurs at:

1 / (2 x pi x 44E-12 x 10E6) = 361Hz for the 10M Ohm bias resistor

1 / (2 x pi x 231E-12 x 2.6E6) = 265Hz for the 2.6M Ohm bias resistor

The -6dB OPA859 buffer is protected from severe overload by series connected very low capacitance (0.3pF) diodes (BAR63-04). These are biased to limit the OPA859 input voltage to between +1V1 and +4V0. This input range limit also prevents the OPA859 from going into saturation, which could cause recovery time distortion issues.

The -26dB buffer is protected by the attenuator, because an OPA859 input signal of +/-1V requires an external signal of +/-20V, which is limited by the input stage TVS diode.

3.3 1M Ohm attenuator PCB

The earlier design study highlighted 2 significant effects caused by FR4 type PCB when used at high impedance and high frequencies, which result in analogue signal distortion:

1. Dielectric absorption
2. The Hook effect, caused by the frequency dependency of dielectric absorption

These are both explained in the following excellent reference:

“Wideband Amplifiers” by Peter Staric and Erik Margan, published by Springer (2006). (Section 5.2)

The graph below is reproduced from Fig 5.2.11 in this reference, and shows the Hook effect caused by FR4 pcb material on a simple high impedance divide by 10 attenuator:

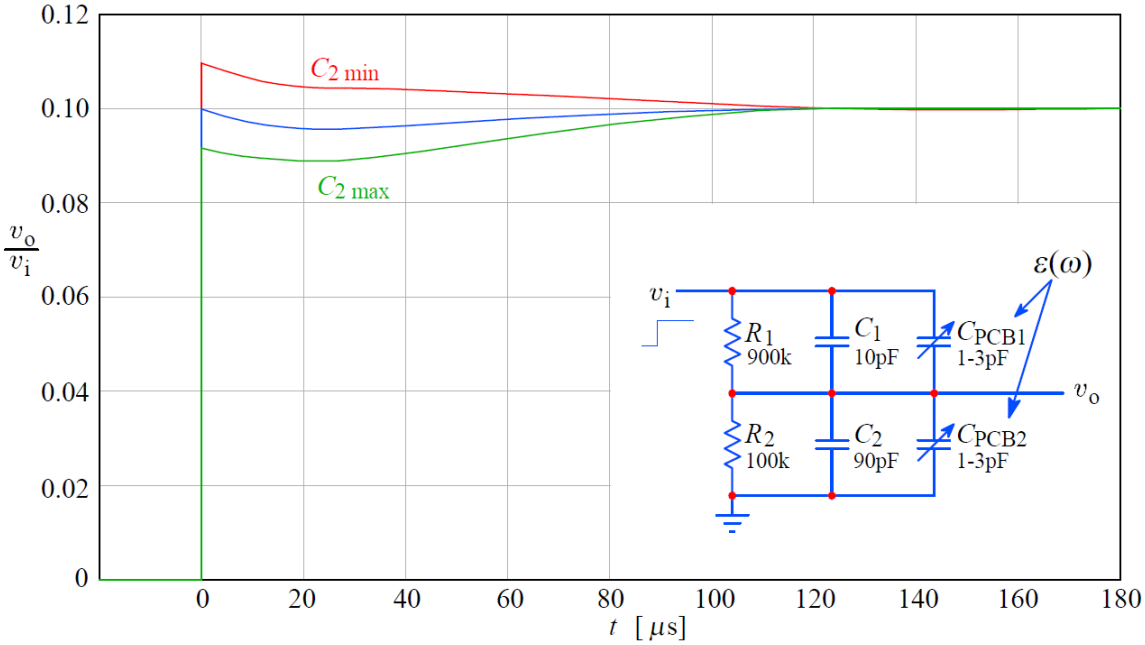


Figure 3: The Hook Effect

This is a significant distortion of the incoming signal and steps must be taken to minimise the effect. The effect is reduced with a pcb material designed to minimise losses and absorption, and typically used for high frequency RF designs, however this costs more than FR4. This issue is discussed further in the section below on PCB design.

3.4 Attenuator Multiplexor

A 4 input GaAs SP4T high power switch type MASW-007813 from MACOM allows selection of any one of the 4 separate attenuator paths. This device is specified for operation from DC to 3GHz, and has a 0.1dB gain compression point of 38dBm.

https://www.macom.com/products/product-detail/MASW-007813-000000

It has 4 control inputs, one for each switch, which are generated by 4 inverting buffers supplied from +5V, type SN74LV540, which outputs 0/+5V levels.

https://www.ti.com/product/SN74LV540A

The 4 control signals are generated by half of a dual 2 to 4 decoder type SN74HCT139 by TI, from 2 control signals S8 and S9. Only one half of this device is used for each channel. It is supplied with +5V, and has 5V CMOS outputs and 3.3V CMOS/TTL inputs.

https://www.ti.com/lit/gpn/sn74hct139

3.5 Low Frequency Attenuator LFA

The low frequency attenuator provides programmable DC offset and gain adjustment, and switched 8Hz high pass filter. The gain control allows the low frequency gain to be precisely matched to any high frequency gain by using a 16 bit multiplying DAC, and a simple calibration process. This avoids the need to provide a manual adjustment to match the low and high frequency gains in an attenuator. It also allows the high frequency attenuators to be AC coupled at all times, which greatly simplifies the design of these attenuators.

The input to the LFA is coupled from the 50 Ohm and 1M Ohm attenuator inputs with series resistors which feed the inputs of a pair of OPA192 buffer amplifiers.

https://www.ti.com/lit/gpn/opa192

The OPA192 has a very high input impedance of 100M Ohms, 1.6pF and an input offset of just +/-50uV maximum. The 2 buffered outputs are connected to an SPDT switch type ADG1436.

https://www.analog.com/media/en/technical-documentation/data-sheets/ADG1436.pdf

This switch is controlled by signal 50R/1MN, which allows selection of either the 1M or 50 Ohm inputs. The output of this switch is fed to the input of another SPDT switch controlled by AC/DCN. This switch can switch between an 8Hz high pass filter, and a direct connection to the difference amplifier stage.

The difference amplifier is implemented as a differential input amplifier using precision 0.1% resistors. The differential inputs are the external signal, and the output of the offset DAC. It subtracts the offset from the wanted signal and drives

the input of the 16 bit multiplying DAC. The offset DAC is an AD5761R with built in reference by Analog Devices. It provides a programmable output of up to +/-10V.

https://www.analog.com/media/en/technical-documentation/data-sheets/ad5761r_5721r.pdf

The gain control 16 bit DAC is type DAC8811 by TI, which multiplies the incoming signal by the programmed 16 bit fractional digital code. The DAC output is a current which is converted to a voltage by another OPA192, which also acts as an output buffer.

https://www.ti.com/lit/gpn/DAC8811

The AD5761R offset DAC also generates a +2.500V reference, which is both buffered and inverted by a pair of OPA2192s to generate +2.500V and -2.500V. The -2.500V reference is added to the output of the gain control DAC, so that it has a fixed +2.500V bias. An OPA2192 buffer is used as a current summing amplifier to generate the low frequency attenuator output. The +2.500V reference is output to provide a pseudo differential output signal ATTENDC.

The buffered low frequency output is combined with the capacitive coupled output of the multiplexor from the AC attenuator, at the input to the LMH6518. The way this is done is critical to the entire design, in order to provide a flat frequency response.

Simulations of this part of the design show that it is essential to have a very wide overlap frequency between the low and high frequency stages. It is relatively easy to set the amplitudes of the 2 signals the same by using the programmable attenuator in the LFA. To obtain an acceptably flat frequency response it is also necessary to minimise the effect of the phase shift in the low and high frequency signals at the high and low frequency roll offs.

By careful component selection, it is possible to set the frequency where the output impedance of one source becomes significantly greater than the other. The source with the lowest impedance then drives the signal alone, and the relative phases do not matter. Simulations have shown that it is possible to obtain an output frequency response with arbitrarily small amplitude tolerance, by careful component value selection. In practice a tolerance of better than the industry accepted norm of +/-1% (+/-0.086dB) is the design aim.

The simulated high frequency response of the LFA is around 1MHz, and the low frequency response of the AC attenuators is below 100Hz, giving at least 4 decades of overlap. This area of the design may require some component value adjustments during the prototype phase.

3.6 Attenuator Output Amplifier

The combined signal from the high frequency attenuators and the LFA is an input to the Digitally Controlled Variable Gain Amplifier, type LMH6518 by TI:

https://www.ti.com/lit/gpn/lmh6518

The negative input is driven by the +2.500V reference generated in the LFA. The positive input is protected from overload by series connected low capacitance diodes.

This device has a SPI interface which allows software to vary the gain between -1.16dB and +38.8dB (range 40dB) with a step size of 2dB. The -3dB bandwidth is 900MHz. It has a programmable low pass filter which allows settings of 20, 100, 200, 350, 650, 750, 900MHz. There are 2 identical differential outputs, so that the same signal can be sent to both main ADCs, allowing interleaved sampling at up to 2GHz.

The differential input impedance is 150k Ohms in parallel with 1.5pF. This makes it easy to drive, although the aim is to keep the source impedance to 50 Ohms or below at high frequencies.

The SPI interface has 3 signals, a clock (SCLK), bidirectional data (SDIO) and a chip select (AMPCSN), which are connected to the control section.

For power estimating, this device consumes a significant amount of power from the +5V supply. Sampling at 1GHz, both channel 1 and 2 devices are on but the auxiliary outputs can be turned off. The current draw is then 170mA maximum each, 340mA total. Sampling at 2GHz only one device needs to be on, but it does need its auxiliary output on. The current draw is then 230mA.

3.7 Attenuator Signal Levels

The following table shows how the system gains are set for each input range.

The sampling ADC differential full scale range is set to either 400mVpp or 500mVpp. See section 4.1 below for details of this.

Note that the input attenuator provides the same 6dB or 26dB attenuation for both 1M Ohm and 50 Ohm inputs.

Input FS Range	Input Atten	MUX FS Output	DVGA Gain	DVGA Gain	ADC Input
+/-50mV	6dB	+/-25mV	18dB	8	+/-200mV
+/-250mV	6dB	+/-125mV	4dB	1.6	+/-200mV
+/-500mV	26dB	+/-25mV	18dB	8	+/-200mV
+/-2.5V	26dB	+/-125mV	4dB	1.6	+/-200mV
+/-5V	26dB	+/-250mV	0dB	1	+/-250mV

The gain settings within the system are versatile enough to allow the implementation of a number of other input full scale ranges.

4 Digital Architecture

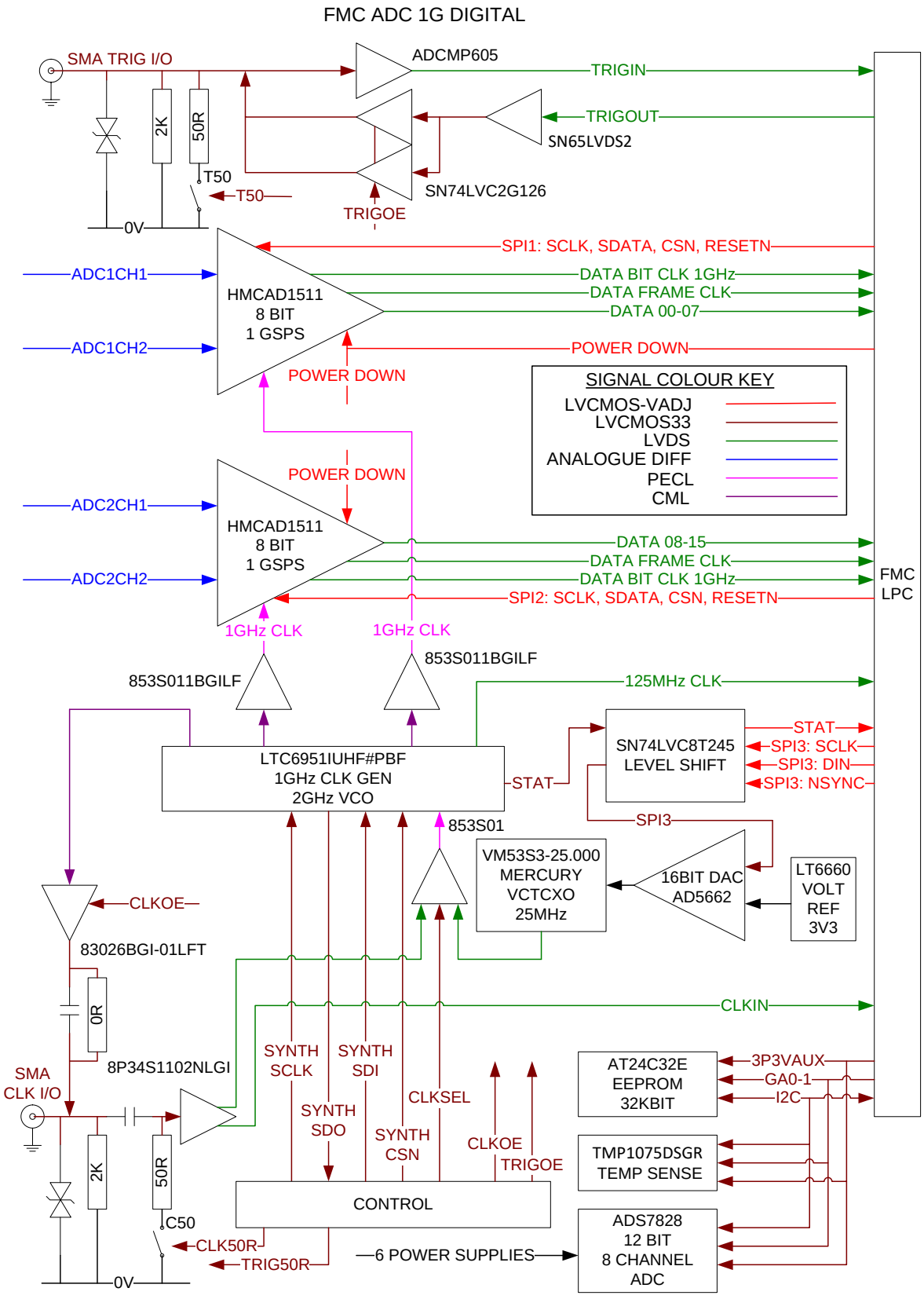


Figure 4: Digital Architecture

4.1 Digital Sampling ADCs

There are 2 HMCAD1511 ADCs specified for 1GHz at 8 bits each.

The sampling can be interleaved by inverting one ADC clock to allow 2GHz sampling of a single input channel. This requires each input channel sends a duplicate of its signal to both ADCs. The LMH6518 attenuator output driver has 2 outputs, each is connected to a different ADC.

The ADC data is output as 8 LVDS data streams directly to the FMC connector, along with an LVDS data frame clock and an LVDS data bit clock, making the data synchronous with the clock and phase aligned.

Each ADC has its own private LVCMOS SPI control connected directly to the FMC bus. There are 4 SPI signals:

1. SCLK clocks the SPI data
2. SDATA is the serial data input to the ADC (no output)
3. CSN is an active low chip select
4. RESETN is an active low SPI interface reset

Both ADCs share a single LVCMOS power down signal, controlled directly by the FMC bus. This is to ensure they both exit power down at exactly the same time instant, so there are no synchronisation issues.

The ADC supports an LVCMOS supply voltage of 1.7 to 3.6V, which is supplied directly from the FMC VADJ supply. This removes the need to fit level shifters, since the LVCMOS digital signals can also be connected directly from the FMC bus to the ADCs. Also see section “Power supply 2V2”.

https://www.analog.com/en/products/hmcad1511.html

The design also supports the HMCAD1520 ADC which is similar, but offers higher resolution at lower sample rates. This device also has lower power dissipation at 490mW total, compared to 710mW total for the HMCAD1511.

https://www.analog.com/en/products/hmcad1520.html

The maximum differential input full scale range is specified as 2.0Vpp typical.

The ADC has 2 ways to adjust the full scale range for smaller inputs:

1. Full scale range adjustment of +/-10% provides fine tuning. This is used with the calibration to correct for variations in system gain due to component tolerances.
2. Programmable gain with 4 bits of control and 2 different modes:
3. Mode 0 allows the gain to be set in 1dB integer increments from 0 to +12dB
4. Mode 1 allows the gain to be set to 1, 1.25, 2, 2.5, 4, 5, 8, 10, 12.5, 16, 20, 25, 32, 50

Increasing the gain reduces the Effective Number of Bits (ENOB), and the specification requires at least 6.5 bits. Excluding spurs the ADC ENOB is 7.9 bits at a gain of 1, and 7.6 bits at a gain of 10. External noise issues may become more significant as the gain is increased, so it is preferred to keep the ADC gain as low as possible.

To match the attenuator output levels described above, the ADC gain is set as follows:

Attenuator output full scale	ADC gain
+/-200mV	10
+/-250mV	8

4.2 Digital Sampling ADC clocks

Each ADC is clocked differentially at up to 1GHz. The device supports LVDS clocking up to 700MHz only, and LVPECL, Sine wave, CMOS at 1GHz, with the requirement that a sine clock must have a differential swing of at least 1.5Vpp.

The synthesiser is Analog Devices LTC6951, which has 5 differential outputs, OUT0-3 are CML, and OUT4 is LVDS. The CML output differential Voltage is specified as 440mV typical, which is not considered to be sufficient to reliably meet the ADC input clock requirement at 1GHz.

https://www.analog.com/en/products/ltc6951.html

The CML ADC clocks are buffered through IC33 and IC36, 853S011BGILF:

https://www.idt.com/eu/en/products/clocks-timing/clock-distribution/clock-buffers-drivers/853s011bi-low-skew1-2differential-25v33v-lvpeclecl-fanout-buffer

These buffers convert the CML level signal to LVPECL, in order to guarantee to meet the ADC clock amplitude requirement.

The SPI programming manual is separate to the data sheet:

https://www.analog.com/media/en/technical-documentation/user-guides/pll_operating_guide_rf_vcos.pdf

To sample at 2GHz, it is necessary to invert one of the clocks. In the following application note, this is done by swapping the differential clock pair signals:

https://www.analog.com/media/en/technical-documentation/user-guides/hmcad1511_2gsps_oscilloscope_solution.pdf

To be able to switch between 1GHz and 2GHz sampling, it is necessary to invert the clock to one ADC, so that each ADC clocks a new sample on alternate edges of the 1GHz clock. The LTC6951 synthesiser has a setting that allows this to be done under software control. This must be done with both ADCs powered down, so that the clock is stable when the ADCs are powered on.

The LTC6951 synthesiser has a status output, which is buffered and fed directly to the FMC bus and the carrier. This status is software configurable to be the logical OR of a number of internal status bits. One of these indicates if the VCO is locked,

so that the carrier can always know if the synthesiser is locked to the reference clock.

4.3 Digital 25MHz Local VCXO

The specification requires that a local 125MHz clock is provided to the FMC bus and carrier. This must be derived from a VCXO controlled by a DAC. The VCXO specified by CERN is a 25MHz oscillator type VM53S3-25.000-2.5/-30+75 made by Mercury:

https://www.mecxtal-europe.com/media/2184/m-s-tcxo-series-datsheet.pdf

The VCXO control voltage is supplied by a 16 bit DAC type AD5662. This has a private SPI interface from the FMC bus which is level shifted by a SN74LVC8T245. The private SPI bus allows the host to phase lock the VCXO to any signal source including the external clock.

https://www.analog.com/en/products/ad5662.html

The DAC reference voltage is supplied by 3.3V reference LT6660.

https://www.analog.com/en/products/lt6660.html

The 25MHz VCXO output is fed to IC35, an 853S01AKILF differential switch, made by IDT (Renesas):

https://www.idt.com/eu/en/products/clocks-timing/clock-distribution/clock-multiplexers-mux/853s01i-21-differential-lvpecl-multiplexer

This switch also receives the external clock in from the SMA connector, and it allows selection of the local 25MHz clock, or the external clock, as the reference for the frequency synthesiser.

4.4 Digital ADC Clock Synthesiser

The synthesiser IC34 is Analog Devices (Linear Technology) part LTC6951. Analog Devices provide a design wizard, and the screen shot below shows the design generated for a 25MHz reference, with outputs 0 and 1 set to 1GHz, and outputs 3 and 4 set to 125MHz.

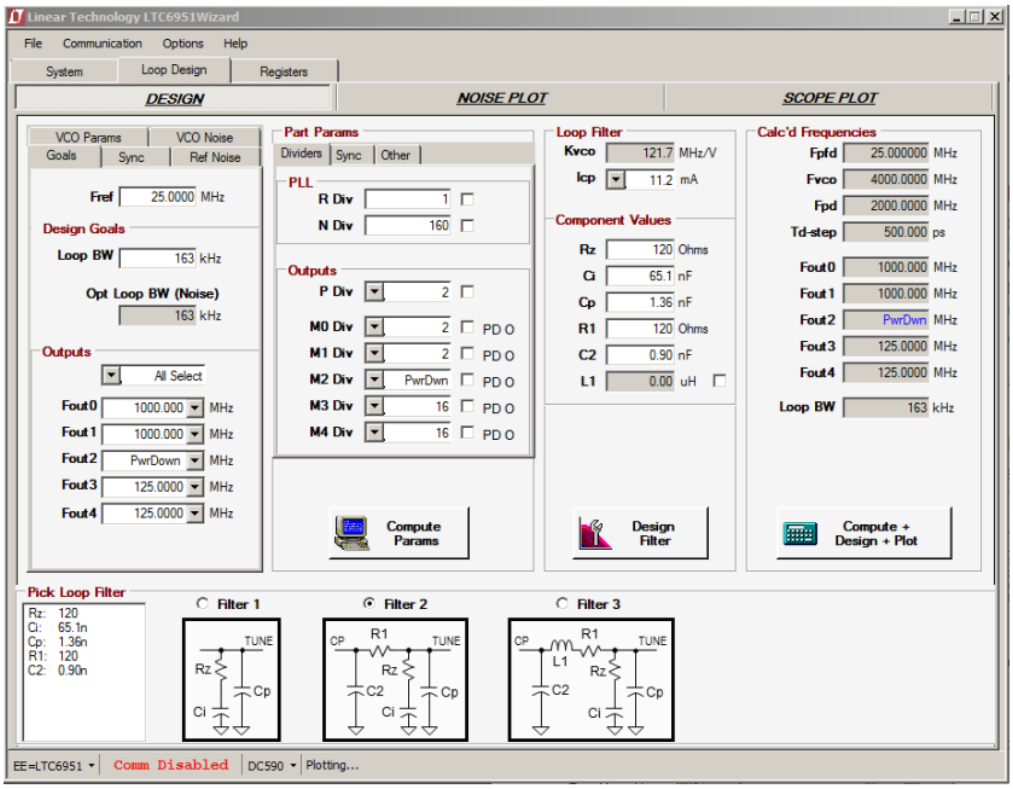


Figure 5: LTC6951 Design Wizard

The filter design is optimised for the 25MHz reference, with a bandwidth of 163kHz. The wizard generates an output noise report, which states the output jitter with an ideal reference clock is as follows:

OUT0 = 138fs	Format = CML	ADC1 Clock
OUT1 = 138fs	Format = CML	ADC2 Clock
OUT3 = 153fs	Format = CML	SMA Output clock at 125MHz
OUT4 = 163fs	Format = LVDS	FMC Output clock to carrier at 125MHz

Note that the optimum filter bandwidth changes slightly with reference frequency. For instance with 125MHz reference the optimum bandwidth is 251kHz. This is only relevant when using an external reference clock, via the SMA connector.

The output dividers offer all powers of 2 and some between, but do not allow selection of any integer divider. So for example it is not possible to have the ADCs clocked at 1GHz, and output 25MHz or 10MHz at OUT3 to the SMA connector.

To synchronise multiple FMC ADC 1G boards, it is recommended that the master clock board should be set to output 125MHz to the SMA connector, and the slave clock boards should be set to an external 125MHz reference clock from the SMA connector.

4.5 Digital External Clock I/O

The external clock signal is protected from overvoltage by a TVS, and can optionally be terminated with 50 Ohms by enabling mosfet switch signal C50. It is AC coupled to the input buffer, an 8P34S1102NLGI by IDT (Renesas):

https://www.idt.com/document/dst/8p34s1102i-datasheet

This device is a 1:2 LVDS buffer, which has very low additive jitter. The external clock signal is attenuated to LVDS levels, to drive the 8P34S1102 buffer. One LVDS output is fed directly to the FMC bus and the carrier, while the other LVDS output is fed to the synthesiser reference source switch.

AC input coupling allows the clock to be supplied either as LVTTL (0 to +2.4V), or from an RF signal source (+/-1.2V).

Synthesiser clock output OUT3, can be output externally at the SMA connector by enabling IC41, 83026BGI-01LF by IDT (Renesas):

https://www.idt.com/document/dst/83026i-01-datasheet

This is a 1:2 differential to LVCMOS buffer with dual 3 state outputs, which are connected in parallel. This part is chosen for low additive phase jitter, and with parallel outputs can drive a 50 Ohm load to 2.6V.

The output is DC coupled to output 0 to +2.4V. A build option is available for AC coupled output (+/-1.2V).

4.6 Digital External Trigger I/O

The external trigger signal is protected from overvoltage by a TVS, and is terminated with a 2K resistor, to allow operation with standard CMOS drivers. It can optionally be terminated with 50 Ohms by enabling mosfet switch signal T50.

The input buffer is ADCMP605 by Analog Devices. This is a fast 1.6ns comparator with LVDS output and pin programmable hysteresis. The hysteresis is set to around 100mV by R296, to ensure that trigger signals with a slow rise time do not cause multiple trigger events.

The LVDS output drives the FMC bus directly with TRIGIN.

https://www.analog.com/media/en/technical-documentation/data-sheets/ADCMP604_605.pdf

The FMC LVDS signal TRIGOUT can be output externally by enabling a pair of SN74LVC2G126DCT buffers, connected in parallel to provide an output current of at least 48mA, in order to drive a 50 Ohm load to 2.4V.

https://www.ti.com/lit/gpn/sn74lvc2g126

4.7 Digital I2C bus

The FMC I2C bus is connected to 3 devices, which are all powered with the FMC supply 3P3VAUX:

1. AT24C32E EEPROM with 32K bits memory. This is required by the FMC standard, and is used to store board identification and other useful information such as calibration data.
2. TMP1075DSGR Temperature sensor. The specification calls for a DS182x one wire temperature sensor. The only part available in a small package is DS1825 and this requires a high data level of at least 2.2V when powered locally. To interface this one wire interface to the FMC bus with VADJ and hence the CMOS high logic level set to 2.2V, requires bus level translation, but the one wire interface is bidirectional, so that knowledge of the transmit and receive function is required. Conclusion: it is very much simpler to implement an I2C sensor. The TMP1075 is available in WSON package which is only 2 x 2 mm.
3. ADS7828 12 bit ADC with 8 inputs, connected to monitor all of the local power supplies.

The I2C addressing is defined for the EEPROM in the FMC standard:

	GA[0..1]	I2C Address for serial 32Kb EEPROM	I2C Addresses for Optional Devices
32Kb EEPROM	00	0b101 0100	0bxxx xx00
	01	0b101 0101	0bxxx xx01
	10	0b101 0110	0bxxx xx10
	11	0b101 0111	0bxxx xx11

To implement these addresses the AT24C32E input A2 is set to 1, A1 is connected to GA0 and A0 is connected to GA1 as specified in the FMC standard.

The TMP1075 also has 3 address pins A2-A0. With A2 connected to 3P3VAUX, and A1 to GA0 and A0 to GA1 the TMP1075 responds at the following 4 addresses:

GA[0..1)	TMP1075 address
00	0b1001100
01	0b1001101
10	0b1001110
11	0b1001111

The ADS7828 has 2 address pins A0, A1. These are attached to GA0 and GA1 so the ADS7828 responds at the following addresses:

GA[0..1)	ADS7828 address
00	0b1001000
01	0b1001001
10	0b1001010
11	0b1001011

This allows up to 4 boards to be fitted into the same FMC system and each to have an independent set of I2C addresses.

https://www.microchip.com/wwwproducts/en/AT24C32E

https://www.ti.com/lit/gpn/TMP1075

https://www.ti.com/lit/gpn/ADS7828

The ADS7828 is connected to attenuated versions of the power supplies as follows:

Channel	Power supply	Attenuation	Comment
0	-11V	6	Attenuated to +3P3VAUX
1	-5V	3	Attenuated to +3P3VAUX
2	+11V	6	Attenuated to 0V
3	+5V	3	Attenuated to 0V
4	+3P3VAUX	2	Attenuated to 0V
5	+3V3	2	Attenuated to 0V
6	+2V2 (VADJ)	2	Attenuated to 0V
7	+1V8	2	Attenuated to 0V

To measure the negative supplies, the attenuator is connected to the +3P3VAUX supply instead of 0V. The negative supplies are connected as follows:

Power supply	**Resistor to ADS7828 input**	**Resistor from ADS7828 input to +3P3VAUX**	**Nominal voltage at ADS7828 input**
-11V	50K00	10K00	+0.916V
-5V	20K00	10K00	+0.533V

5 Control Architecture

5.1 Control Shared SPI bus

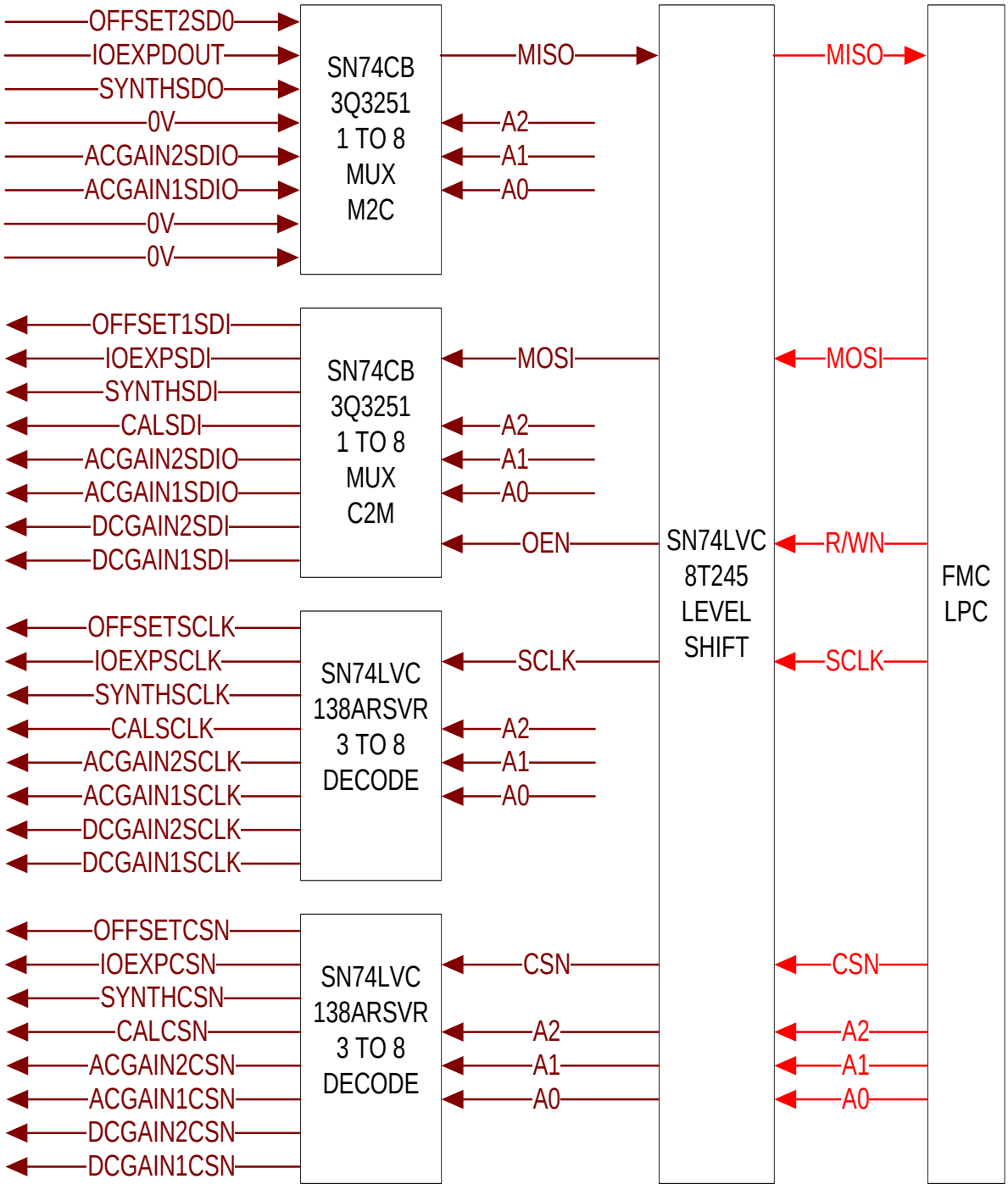


Figure 6: SPI Architecture

The shared SPI bus consists of 8 LVCMOS signals on the FMC bus:

Signal	In/Out	Description
A0	In	Address bit 0
A1	In	Address bit 1
A2	In	Address bit 2
CSN	In	Global chip select
R/WN	In	R/-W
MISO	Out	SPI data from peripheral
MOSI	In	SPI data to peripheral
SCLK	In	SPI clock

Signal R/WN is only set high to read when addressing either of the LMH6518 output amplifiers, because only these devices have a bidirectional data port. This signal must be set low to write, when other devices are addressed.

A0-2 and CSN drive a SN74LVC138 3 to 8 decoder, which generates 8 active low chip selects. These are used to decode one of the 8 devices on the shared SPI bus:

A2-0	CHIP SELECT	Description
0	DCGAIN1CSN	Channel 1 low frequency gain DAC: DAC8811
1	DCGAIN2CSN	Channel 2 low frequency gain DAC: DAC8811
2	ACGAIN1CSN	Channel 1 output amplifier: LMH6518
3	ACGAIN2CSN	Channel 2 output amplifier: LMH6518
4	CALCSN	Calibration DAC: AD5683
5	SYNTHCSN	Clock synthesiser: LTC6951
6	IOEXPCSN	28 port I/O expander: MAX7301
7	OFFSETCSN	Ch1 & Ch2 DC Offset DACs in series: AD5761

A0-2 and SCLK drive a SN74LVC138 3 to 8 decoder, which generates 8 serial data clocks. These are each used to clock one of the 8 devices on the shared SPI bus:

A2-0	CHIP SELECT	Description
0	DCGAIN1SCLK	Channel 1 low frequency gain DAC: DAC8811
1	DCGAIN2SCLK	Channel 2 low frequency gain DAC: DAC8811
2	ACGAIN1SCLK	Channel 1 output amplifier: LMH6518
3	ACGAIN2SCLK	Channel 2 output amplifier: LMH6518
4	CALSCLK	Calibration DAC: AD5683
5	SYNTHSCLK	Clock synthesiser: LTC6951
6	IOEXPSCLK	28 port I/O expander: MAX7301
7	OFFSETSCLK	Ch1 & Ch2 DC Offset DACs in series: AD5761

A0-2 and R/WN control an 8 way multiplexor, which connects each of the 8 devices on the shared SPI bus to MOSI. The signal R/WN enables the multiplexor when low, to enable data writing from carrier to the I/O device. It must be set high to enable read back from the ACGAIN output amplifiers.

A2-0	CHIP SELECT	Description
0	DCGAIN1SDI	Channel 1 low frequency gain DAC: DAC8811
1	DCGAIN2SDI	Channel 2 low frequency gain DAC: DAC8811
2	ACGAIN1SDIO	Channel 1 output amplifier: LMH6518
3	ACGAIN2SDIO	Channel 2 output amplifier: LMH6518
4	CALSDI	Calibration DAC: AD5683
5	SYNTHSDI	Clock synthesiser: LTC6951
6	IOEXPSDI	28 port I/O expander: MAX7301
7	OFFSET1SDI	Ch1 DC Offset DACs: AD5761

A0-2 control an 8 way multiplexor, which connects each of the 8 devices on the shared SPI bus to MISO, for data read back from those devices which support this feature.

A2-0	CHIP SELECT	Description
0	0V	Not supported
1	0V	Not supported
2	ACGAIN1SDIO	Channel 1 output amplifier: LMH6518
3	ACGAIN2SDIO	Channel 2 output amplifier: LMH6518
4	0V	Not supported
5	SYNTHSDO	Clock synthesiser: LTC6951
6	IOEXPDOUT	28 port I/O expander: MAX7301
7	OFFSET2SDO	Ch1 DC Offset DACs: AD5761

Note that the 2 offset DACs are connected in a daisy chain, with channel 1 DAC first in the chain.

5.2 Control 28 port I/O expander

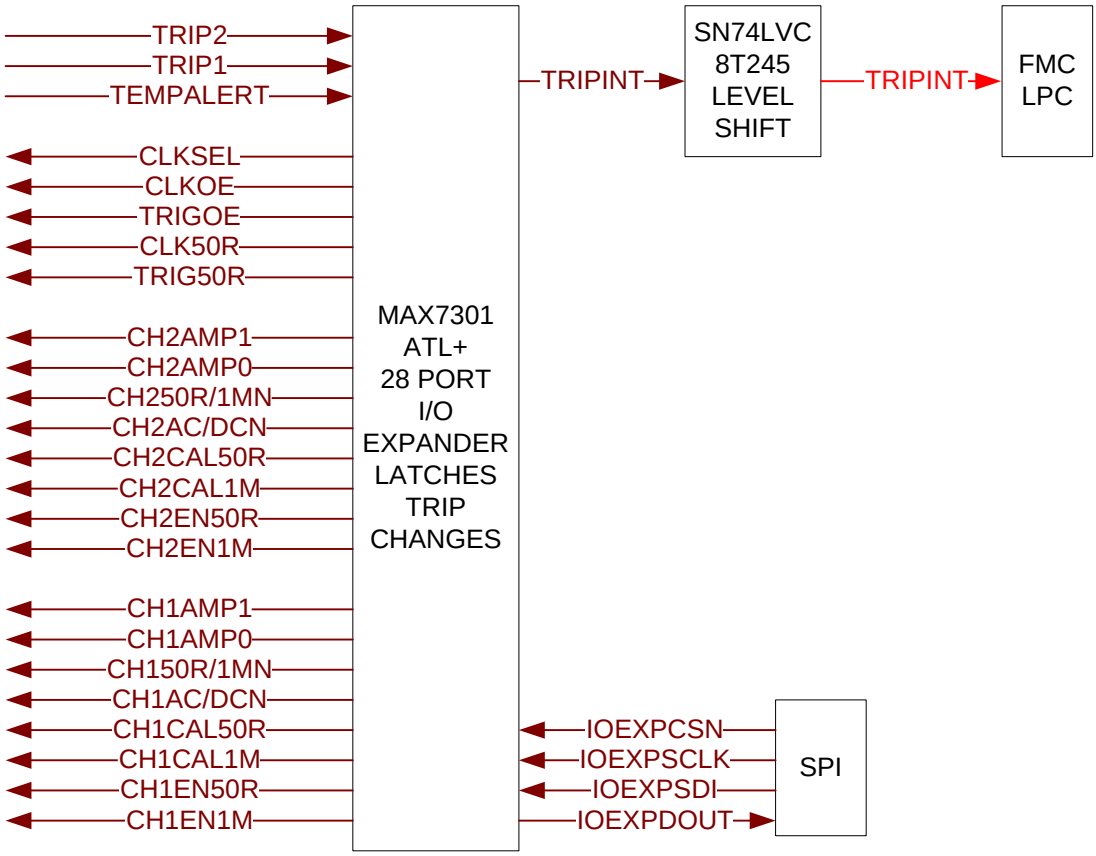


Figure 7: I/O Expander Architecture

A MAX7301 28 port I/O expander is controlled by the shared SPI bus. It outputs all of the bit level control signals and an interrupt to the FMC bus. It receives the thermal trip signals from each input channel on ports which have transition detection logic (P24-P30). The interrupt output can be generated automatically when an input transition is detected. Software can then determine which trip caused the interrupt.

The I/O bits are numbered 4 to 31 in the data sheet.

https://www.maximintegrated.com/en/products/interface/controllers-expanders/MAX7301.html

The 28 I/O bits are defined as follows:

I/O Bit	Net name	Description
4	CH1EN1M	Ch1 external signal to 1M input
5	CH1EN50R	Ch1 external input to 50 Ohm input
6	CH1CAL1M	Ch1 CAL to 1M input
7	CH1CAL50R	Ch1 CAL to 50 Ohm input
8		Unused
9	CH1AC/DCN	Ch1 high = 8Hz high pass filter, low = no filter
10	CH150R/1M	Ch1 high = 50 Ohm input, low = 1M Ohm input to LFA
11	CH1AMP0	Ch1 multiplexor bit 0
12	CH1AMP1	Ch1 multiplexor bit 1
13	CH2EN1M	Ch2 external signal to 1M input
14	CH2EN50R	Ch2 external input to 50 Ohm input
15	CH2CAL1M	Ch2 CAL to 1M input
16	CH2CAL50R	Ch2 CAL to 50 Ohm input
17		Unused
18	CH2AC/DCN	Ch2 high = 8Hz high pass filter, low = no filter
19	CH250R/1M	Ch2 high = 50 Ohm input, low = 1M Ohm input to LFA
20	CH2AMP0	Ch2 multiplexor bit 0
21	CH2AMP1	Ch2 multiplexor bit 1
22	TRIG50R	External trigger input 50 Ohm termination when high
23	CLK50R	External clock input 50 Ohm termination when high
24	TRIGOE	External trigger output enable when high
25	CLKOE	External clock output enable when high
26	CLKSEL	External clock synthesiser reference when high. 25MHz local VCXO synthesiser reference when low
27		Unused
28	TEMPALERT	Input: I2C Temperature sensor Alert
29	TRIP1N	Input: Ch1 input attenuator thermal trip when low
30	TRIP2N	Input: Ch2 input attenuator thermal trip when low
31	TRIPINT	Trip interrupt to the FMC bus

5.3 Calibrator

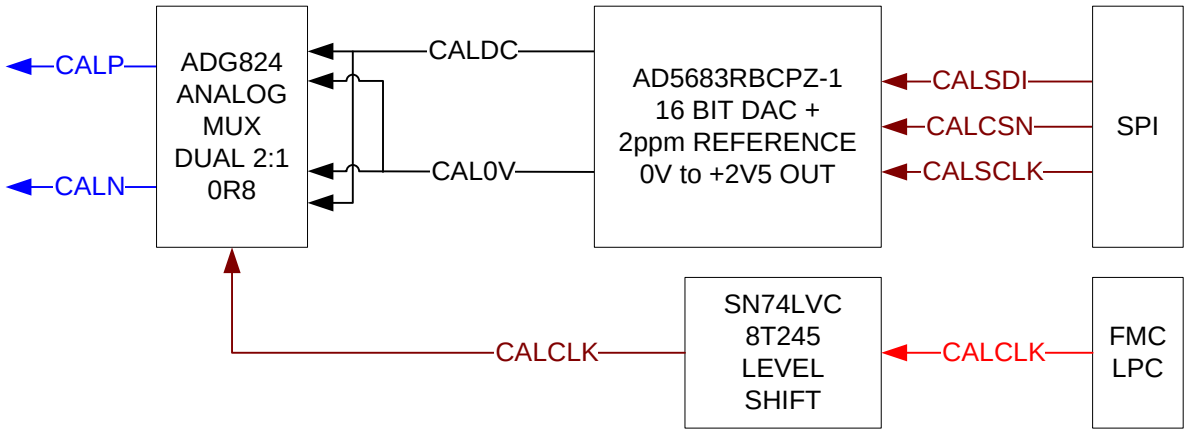


Figure 8: Calibrator

The calibration signal generator consists of an AD5683R 16 bit DAC with SPI control, and an ADG824 dual analog switch. The calibration voltage of 0 to +2.500V is selected by programming the DAC. The analog switch allows a clock from the FMC master to connect this calibration voltage either to the CALP output with CALCLK high, or the CALN output with CALCLK low. This generates a square wave calibration signal with amplitude set by the DAC, and frequency set by the FMC master clock CALCLK. The CALCLK can be set constantly high or low for DC calibrations.

It is recommended to perform all calibrations with CALCLK at or below 1MHz, as the calibration system has limited bandwidth, and to use an amplitude of +1.00V or lower, to minimise dissipation when calibrating the 50 Ohm input.

It is possible to generate a custom calibration waveform using the calibration DAC, if required.

https://www.analog.com/media/en/technical-documentation/data-sheets/AD5683R_5682R_5681R_5683.pdf

https://www.analog.com/en/products/adg824.html

A fundamental area of the design is the separation of the AC and DC input paths. It is essential that the DC gain is calibrated correctly for each AC gain setting, in order to guarantee waveform fidelity. This involves generating a low frequency calibration square wave, and adjusting the DC path gain for optimum square wave signal quality.

Both external input relays must be disabled when performing a calibration.

6 Power Supplies

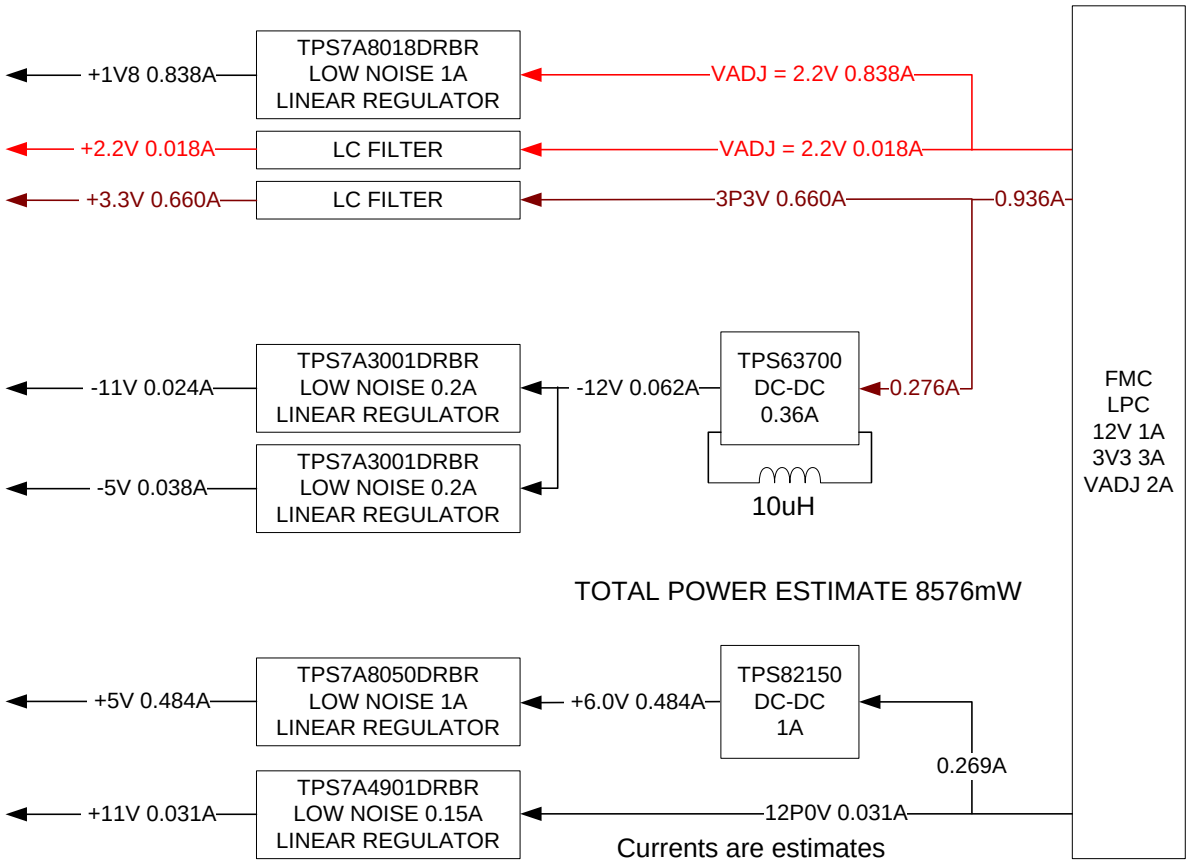


Figure 9: Power Architecture

6.1 Power supply 1V8

This is generated by a low noise linear regulator, type TPS7A8018 from the VADJ supply, which is set to 2.2V to minimise dissipation. Estimated current draw is 0.8A, and dissipation in the regulator is estimated at 320mW.

https://www.ti.com/lit/gpn/TPS7A80

6.2 Power supply 2V2

This is generated by filtering the FMC VADJ supply with an LC filter. Estimated current draw is 0.08A.

The preferred level of VADJ is 2.2V in order to minimise power dissipation. The design will accept 2.5 VADJ, at a slight increase in power dissipation in the 1V8 regulator. The estimated current draw is 838mA, so the 1V8 regulator power dissipation is increased from:

VADJ = 2.2V: 0.4V * 838mA = 335.2mW to

VADJ = 2.5V: 0.7V * 838mA = 586.6mW, an increase of 251.4mW.

A constraint on VADJ is not a design specification.

Both ADCs have the 2V2 power supply connected to ADC supply OVDD (pin 33), the digital CMOS inputs supply voltage. This pin supports supplies in the range 1.7V to 3.6V. The ADC logic inputs switching levels are:

VADJ V	Low level input V	High level input V
2.2	0.44	1.76
2.5	0.50	2.00

This supply is used as the FMC logic level reference by all of the level shifters which shift the FMC LVCMOS signals to internal signal levels. See “ANSI/VITA 57.1-2019” Rule 6.4:

“IO signals designated LAxx_y and HAxx_y shall be driven by the common VADJ supply.”

6.3 Power supply 3V3

This is generated by filtering the FMC 3P3V supply with an LC filter. Estimated current draw is 0.66A.

6.4 Power supply 5V0

This is generated by a low noise linear regulator, type TPS7A8050 from the 6V supply. Estimated current draw is 0.484A, and dissipation in the regulator is estimated at 484mW.

https://www.ti.com/lit/gpn/tps7a80

The 6V supply is generated by a monolithic DCDC type TPS82150 from the FMC 12V supply. Estimated current draw is 0.269A.

https://www.ti.com/lit/gpn/TPS82150

6.5 Power supply -11V0

This is generated by a low noise linear regulator, type TPS7A3001 from the -12V supply. Estimated current draw is 0.024A, and dissipation in the regulator is estimated at 24mW.

https://www.ti.com/lit/gpn/tps7a30

The -12V supply is generated by an inverting DCDC type TPS63700 from the FMC 3.3V supply. Estimated current draw is 0.276A.

https://www.ti.com/lit/gpn/TPS63700

6.6 Power supply +11V0

This is generated by a low noise linear regulator, type TPS7A4901 from the FMC 12V supply. Estimated current draw is 0.031A, and dissipation in the regulator is estimated at 31mW.

https://www.ti.com/lit/gpn/TPS7A49

6.7 Power FMC Total Power Draw Estimate

With the FMC VADJ supply set to 2.2V, the estimated current draw is 0.856A and power is 1.883W.

The FMC 3P3V estimated current draw is 0.936A and power is 3.089W.

The FMC 12P0V estimated current draw is 0.300A and power is 3.600W.

The total FMC power draw estimate is:

1.883 + 3.089 + 3.600 = 8.572 Watts

This exceeds the specified requirement of 7 Watts maximum, but is less than the FMC standard requirement of 10 Watts maximum.

7 FMC BUS

7.1 FMC LPC Signal summary

There are 2 versions of the FMC connector: High and Low pin count (LPC). The specification requires the use of the LPC connector, which is defined with the following signals:

Signal Positive	Signal Negative	Description
VREF_A_M2C	none	Optional reference Voltage for LAxx from mezzanine
PG_C2M	none	Power Good from carrier
PRSNT_M2C_L	none	Mezzanine module present
GBTCLK0_M2C_P	GBTCLK0_M2C_N	Multi-gigabit clock from mezzanine
DP0_C2M_P	DP0_C2M_N	Multi-gigabit data pair from carrier
DP0_M2C_P	DP0_M2C_N	Multi-gigabit data pair from mezzanine
CLK0_M2C_P	CLK0_M2C_N	Clock 0 from mezzanine to carrier
CLK1_M2C_P	CLK0_M2C_N	Clock 1 from mezzanine to carrier
LA00_P_CC	LA00_N_CC	User defined, can be used as a clock
LA01_P_CC	LA01_N_CC	User defined, can be used as a clock
LA02_P to LA16_P	LA02_N to LA16_N	User defined, 15 pairs
LA17_P_CC	LA17_N_CC	User defined, can be used as a clock
LA18_P_CC	LA18_N_CC	User defined, can be used as a clock
LA19_P to LA33_P	LA19_N to LA33_N	User defined, 15 pairs
TCK, TDI, TDO, TMS, TRST_L	none	JTAG
SCL, SDA	none	I2C
GA0 to GA1	none	I2C geographical address
VADJ	none	Adjustable power from carrier, 2A max
3P3V	none	3V3 power from carrier, 3A max
12P0V	none	12V0 power from carrier, 1A max

To summarise the signals of interest to this design:

1. 34 User defined data pairs, including 4 optional clock pairs. Each pair can be split into 2 single ended user defined signals. CMOS Signal level = VADJ

2. 2 dedicated clock pairs from mezzanine to carrier
3. A single I2C bus
4. A full duplex multi gigabit interface with dedicated clock

7.2 FMC signal mapping

The table below lists the mapping between FMC user defined signals and FMC signals:

FMC Pair	LVDS / CMOS	USER Pair	DIR	Description
LA00_CC	LVDS	ADC1: LCLK	M2C	ADC1 Bit Clock
LA01_CC	LVDS	TRIGOUT	C2M	Trigger Output
LA02	LVDS	ADC1: D1A	M2C	ADC1 data 1A
LA03	LVDS	ADC1: D1B	M2C	ADC1 data 1B
LA04	LVDS	ADC1: D2A	M2C	ADC1 data 2A
LA05	LVDS	ADC1: D2B	M2C	ADC1 data 2B
LA06	LVDS	ADC1:FCLK	M2C	ADC1 Frame Clock
LA07	LVDS	ADC1: D3A	M2C	ADC1 data 3A
LA08	LVDS	ADC1: D3B	M2C	ADC1 data 3B
LA09	LVDS	ADC1: D4A	M2C	ADC1 data 4A
LA10	LVDS	ADC1: D4B	M2C	ADC1 data 4B
LA11_P	CMOS	ADC1:CSN	M2C	ADC1 Chip select
LA11_N	CMOS	ADC1:SDATA	M2C	ADC1 Serial Data
LA12_P	CMOS	ADC1:SCLK	M2C	ADC1: Serial Clock
LA12_N	CMOS	ADC1:RESETN	M2C	ADC1: ResetN
LA13_P	CMOS	ADC:PD	M2C	ADC1&2: Power Down
LA13_N	CMOS	DACCSN	M2C	DAC Chip Select_N
LA14_P	CMOS	DACSCLK	M2C	DAC Serial Clock
LA14_N	CMOS	DACDIN	M2C	DAC Data In
LA15_P	CMOS	FMCCALCLK	M2C	CAL Clock
LA15_N	CMOS	FMCTRIPINT	M2C	Trip Interrupt
LA16_P	CMOS	FMCCLKSYNC	M2C	Clock Sync
LA16_N	CMOS	FMCCLKSTAT	M2C	Clock Status
LA17_CC	LVDS	ADC2: LCLK	M2C	ADC2 Bit Clock
LA18_CC	LVDS	TRIGIN	M2C	Trigger Input
LA19	LVDS	ADC2: D1A	M2C	ADC2 data 1A

LA20	LVDS	ADC2: D1B	M2C	ADC2 data 1B
LA21	LVDS	ADC2: D2A	M2C	ADC2 data 2A
LA22	LVDS	ADC2: D2B	M2C	ADC2 data 2B
LA23	LVDS	ADC2: FCLK	M2C	ADC2 Frame Clock
LA24	LVDS	ADC2: D3A	M2C	ADC2 data 3A
LA25	LVDS	ADC2: D3B	M2C	ADC2 data 3B
LA26	LVDS	ADC2: D4A	M2C	ADC2 data 4A
LA27	LVDS	ADC2: D4B	M2C	ADC2 data 4B
LA28_P	CMOS	ADC2:CSN	M2C	ADC2 Chip select
LA28_N	CMOS	ADC2:SDATA	M2C	ADC2 Serial Data
LA29_P	CMOS	ADC2:SCLK	M2C	ADC2: Serial Clock
LA29_N	CMOS	ADC2:RESETN	M2C	ADC2: ResetN
LA30_P	CMOS	FMCSCLK	M2C	SPI Serial Clock
LA30_N	CMOS	FMCMOSI	M2C	SPI MOSI
LA31_P	CMOS	FMCMISO	C2M	SPI MISO
LA31_N	CMOS	FMCWRN	M2C	SPI WriteN
LA32_P	CMOS	FMCCSN	M2C	SPI Chip SelectN
LA32_N	CMOS	FMCA2	M2C	SPI A2
LA33_P	CMOS	FMCA1	M2C	SPI A1
LA33_N	CMOS	FMCA0	M2C	SPI A0
CLK0	LVDS	CLK125	M2C	125MHz reference clock
CLK1	LVDS	CLKIN	M2C	External clock input

Notes:

1. ADC FCLK is mapped between D2B and D3A because it is treated as clocked data, and this is where it is located on the ADC HMCAD1511 chip pin out. So this mapping aids pcb routing.
2. ADC differential pairs LCLK, FCLK, D1-D4 are routed between the ADC chip and FMC connector with length matching to within 0.50mm.

8 PCB Layout

The single width mezzanine module dimensions are defined in the FMC standard with the drawing shown below:

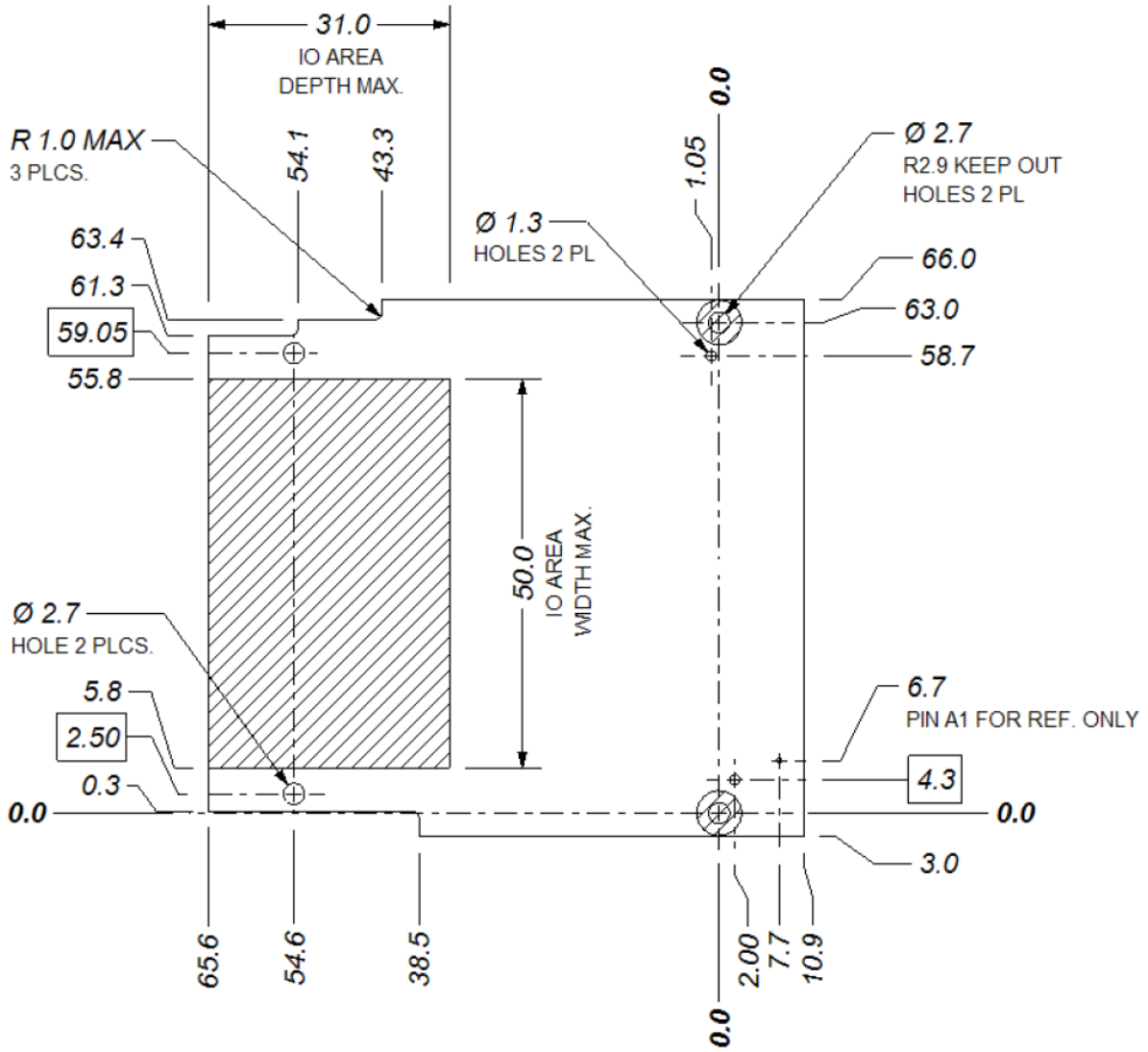
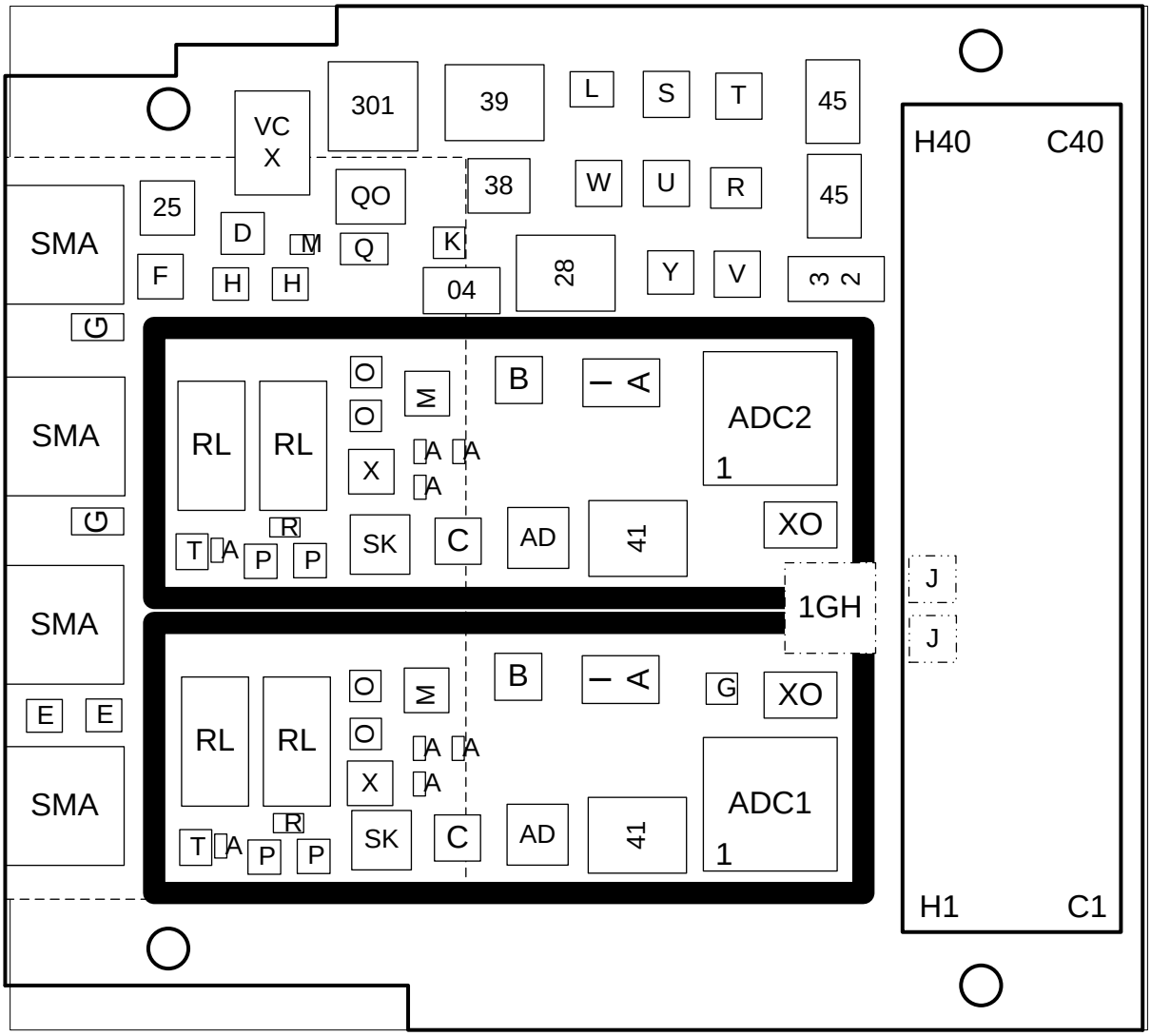


Figure 10: FMC PCB Dimensions

FMC ADC 1G PCB



FMC_ADC_1G PRELIMINARY COMPONENT PLACEMENT
See preliminary part list for component identifiers

Figure 11: FMC ADC 1G PCB Component Placement

This is a rough placement to scale of components on the pcb to show the component density. Only the LTC6951IUHF and the two 853S011BGILF clock buffers have been placed on the bottom, in dashed outline, because they have to be in this location near and equidistant from the main ADCs. There is scope to place a number of other non-critical components, with a height of 1mm or less, on the bottom of the pcb.

The pin 1 locations for both the ADCs and the FMC connector are shown to help illustrate the routing paths between them, and the FMC pin allocation order for ADC signals.

A significant concern for this design is power dissipation. To help prevent hot spots, and spread heat as much as possible a pcb with a heavy dual 2oz copper centre is used. High dissipation components inside the shields have thermal bridging material, to conduct heat up to the shield top cover. The pcb will require a minimum airflow to prevent overheating.

The high impedance RF circuits require a low loss pcb dielectric, with much better performance than standard FR4. The table below lists the proposed layer stack up, and low loss dielectric:

Layer	Function	Material	Min spacing	Notes
1 = TOP	Signal + RF	1oz copper	89um	
	Dielectric	FR408		
2	GROUND	1oz copper	89um	Solid plane
	Dielectric	FR408		
3	Signal + RF	1oz copper	89um	
	Dielectric	FR408		
4	GROUND	2oz copper	355um	Solid plane
	Dielectric	FR4		
5	GROUND	2oz copper	355um	Solid plane
	Dielectric	FR408		
6	Signal NO RF	1oz copper	89um	
	Dielectric	FR408		
7	POWER SPLIT	1oz copper	89um	Multiple power supplies routed as split planes
	Dielectric	FR408		
8 = BOT	Signal NO RF	1oz copper	89um	

While high performance dielectric is not required between layer 5 and 8 for performance reasons, the stack up must be symmetrical to avoid warping issues due to different rates of expansion.

The proposed dielectric material to use for a first trial is FR408 made by Isola:

https://www.isola-group.com/products/all-printed-circuit-materials/fr408/

This epoxy laminate has low dielectric constant (Dk) and low dissipation factor (Df), as well as high temperature resistance for lead free solder.

Tg = 180˚C, Td = 360˚C, Dk = 3.67, Df = 0.012

If dielectric problems are identified during the prototype trial, then trials of higher performance materials may be required.

Guard rings or flood fill are required around all high impedance components, to minimise the dielectric absorption effect.

The use of 2oz copper for the centre ground planes increases the minimum through via clearance on these planes 2oz to 220um to meet manufacturing requirements.

The layout is expected to use buried and blind vias. Apart from the obvious layout issues these significantly help with reducing RF attenuation and stubs.

8.1 Photos - FM582 | Sundance Image Gallery

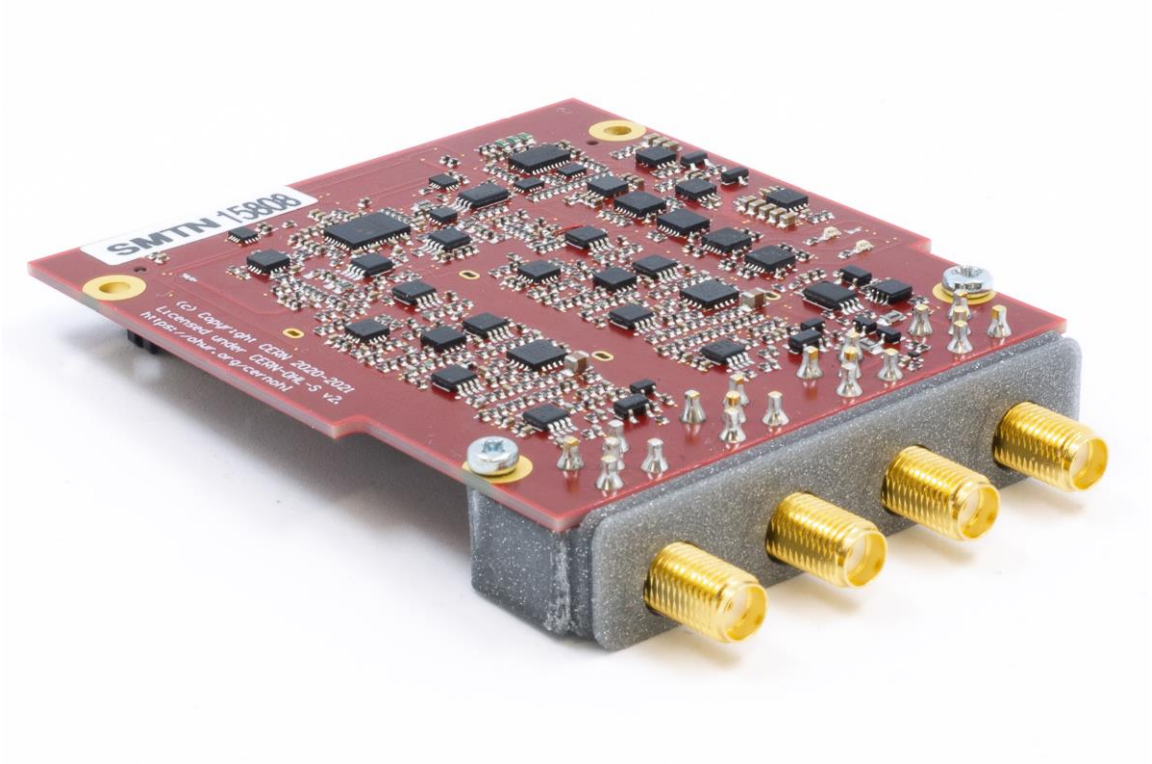


Figure 12 - FM582 bottom

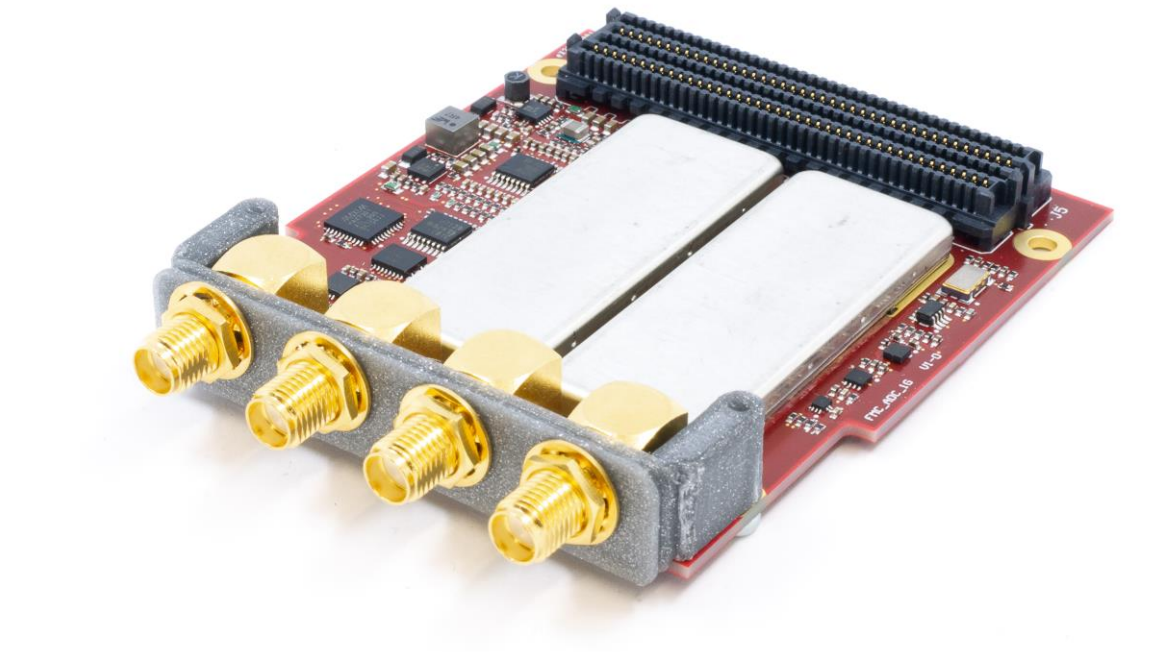


Figure 13: FM582 top