PXIe-700 FPGA BOARD

User Guide

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REVISION HISTORY

Revision	Comments	Originator	Date
1.0	Initial Release	Stephen Malchi	Aug 25th, 2016
1.1	Added VADJ details	Stephen Malchi	Sep 18th, 2016
1.2	Updated Flash features and errors	Stephen Malchi	Sep 30th, 2016
1.3	Updated pin out table	Stephen Malchi	Dec 2nd, 2016
1.4	Added DDR3 Memory details	Stephen Malchi	Jun 13th, 2017
1.5	Updated Rev 4.0 Changes	Stephen Malchi	Nov 10th, 2017
1.6	Updated clock pinout	Stephen Malchi	Dec 10th, 2017
1.7	Added J5 pinout	Stephen Malchi	Jan 21st, 2018

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1 INTRODUCTION

PXIe-700 is a powerful FPGA board in the ruggedized PXIe form factor. The board is based on the Xilinx Kintex-7 FPGA (XC7K410T-1FFG900C) with interface to 4 lanes of Gen2 PCIe, 2 GB of DDR3 memory attached to 2 banks. It includes an HPC FMC site and SFP+ interface. It fully complies with PXIe standard.

1.1 Hardware features

The hardware has the following features:

1. Kintex-7 FPGA (XC7K325T-1FFG900C or XC7K410T-1FFG900C) (optional faster speed grades).
2. 4 lanes of PCIe Gen 2.0 using hard core or Gen 3.0 interface to host with custom IP cores
3. PXI control signals for control and instrumentation support
4. SFP+ cage to provide 10Gb Ethernet using third party IP cores
5. HPC FMC connector with 10 high speed serial links, 2 differential clocks, 68 LVDS pairs, and 8 single-ended signals
6. Two banks of DDR3 SDRAM memory, each 1GB deep and 32-bit wide
7. 128MB flash with multi-boot capability
8. Clock resources to support White Rabbit extreme-precision time protocol via SFP+ fiber

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2 BOARD DESCRIPTION

2.1 PXIe-700 Block Diagram and Pictures

The following diagram shows the major blocks of PXIe-700:

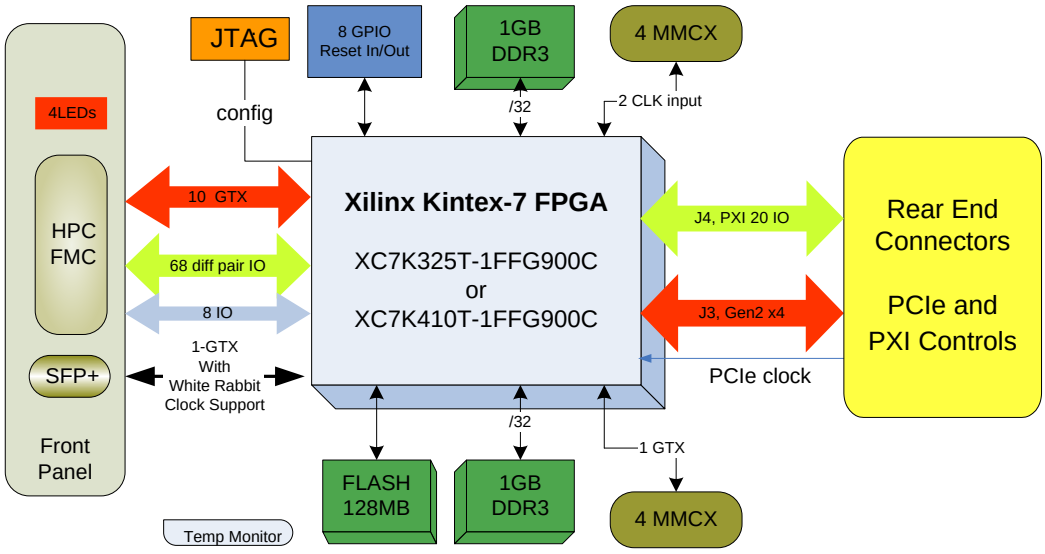

Figure 1: PXIe-700 Block Diagram

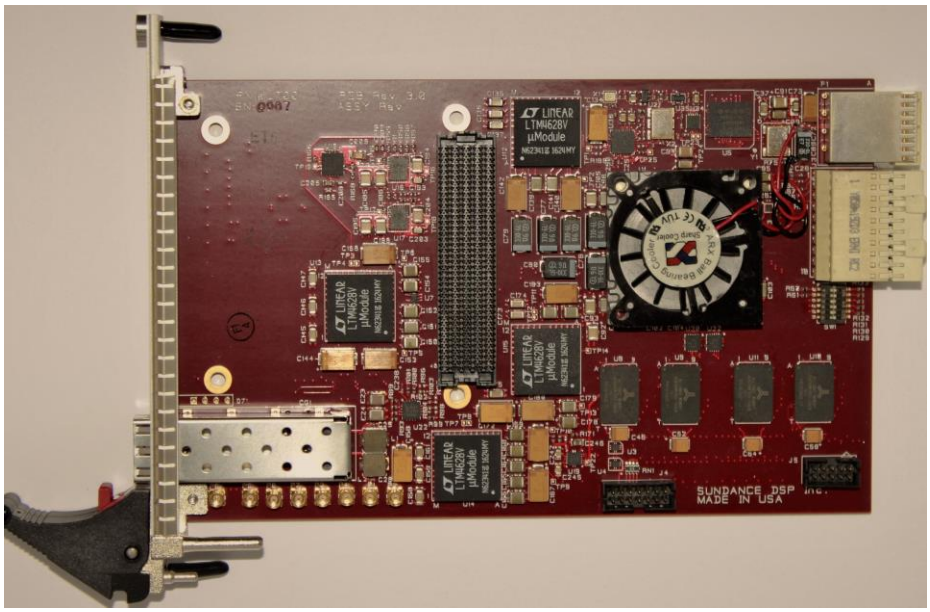

Figure 2: PXIe-700 frontal image

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2.2 BPI FLASH Memory

The board has 128MB of BPI flash memory for storing FPGA bitstreams or software storage.

- Part number: PC28F00AP30TF (micron)
- Supply voltage: 2.5v
- Data rate: up to 33 MHz

When plugged into a PCIe host the board is enumerated within 100ms and the FPGA needs to be configured within 100ms. The BPI flash provides fast FPGA configuration.

Multiple bitstreams can be stored in the BPI flash memory. The two most significant address bits (A25, A24) of the flash are connected to DIP switch SW1 positions 1 and 2. 1 of the 4 bitstreams can be configured by setting the DIP switch.

2.3 Xilinx FPGA

The module is populated with a Xilinx Kintex-7 (FFG900 package) FPGA. The FPGA exists at the heart of every I/O into and out of the module. Various interfaces are available to the FPGA from which data is fed for processing, after which the processed data can be passed to the outside world via any of the interfaces.
The following interfaces are available on the FPGA:

1. Four-lanes of PCIe interface Gen 2.0 using hardcore or Gen 3.0 if using PCIe softcore for data transfer between the FPGA and the host.
2. High Pin Count (HPC) FMC for IO daughter cards.
3. DDR3 memory interface two banks.
4. The FPGA implements 12 Multi-Gigabit Transceivers. These are routed to FMC connector (x10), SFP+ (x1) and one transceiver is connected to MMCX connectors.

2.4 Memory

Two banks of 32-bit DDR3 memory is provided on this board. A total of 2GB SDRAM is attached to this interface for data storage.

The DDR3 memory used on this board is **MT41J64M16JT-15E** or **AS4C64M16D312BCN**

IP core to access the memory can be provided, which will provide read and write access to the memory through host API.

2.5 GTX (High Speed Transceivers)

The FPGA has a total of 16 GTX's. They are used to provide various interfaces on the board which is shown in the table below

GTX's	Connector	Interface
4	PXIe (J2)	PCIe
10	FMC (J1)	User
1	SFP+	User

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1	MMCX	User

Table 1 - High Speed Transceivers

2.6 HPC FMC

The board has an HPC FMC connector for IO daughter cards. A total of 144 IO's are connected to the FPGA out of which 136 IO's can be used as 68 differential pairs and 8 IO's are single ended. There are two differential clocks pins connected to the FPGA.

As mentioned in section 2.5, 10 high speed serial links from the FPGA are available on this connector.

Note: Please see appendix for pinout.

2.7 LEDs

There are 6 LEDs present on this board. Their function and power on default values is described below:

LED	USAGE	Power ON Default
D1	FPGA/DONE	OFF
D2	FMC_PG_C2M	ON
D3	USER	OFF
D4	USER	OFF
D5	USER	OFF
D6	USER	OFF
D7	USER	OFF

Table 2 – LEDs

Note: D7 is optional and populated instead of D3 and D4.

Note: Rev 3.0 of the board comes up with D3 – D6 as ON when it should be OFF on power up.

2.8 Switches

There is one switch, SW1, on the component side of the board. It has the following settings:

SW1	Control
1	Flash_25
2	Flash_24
3	Factory use

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4	Factory use
5	Factory use
6	Not used

Table 3 - Switch (SW1)

Pins 1 and 2 are connected to Flash address pins and are used to select the configuration bit-stream start address. A total of 4 bitstream can be stored and used for FPGA configuration. Pins 3 to 5 should always be set to OFF, ON, OFF as set by the factory. This board only uses Master BPI x16 mode as it has 16-bit Fast parallel NOR Flash connected to the FPGA.

2.9 Clocks

This board requires several clocks for FPGA and high-speed serial transceivers. There are 6 clock sources available:

1) Clock provided by the PCIe Interface
2) 66.6 MHz FPGA_EMC clock for FPGA configuration from Flash
3) A Voltage-Controlled Crystal Oscillator providing a tunable 125MHz clock via CDCM61004 for:
    a. GTXs
    b. FPGA Logic
4) A second VCXO with independent control voltage for use in White Rabbit extreme-precision clock distribution protocol
5) MMCX connectors to provide external clock for user application
6) External Ref Clock for Transceivers via MMCX connectors

A low jitter clock generator from TI CDCM61004 is used to provide 3 clocks for FPGA logic and GTX's.
http://www.ti.com/lit/ds/symlink/cdcm61004.pdf

The output frequencies can range from 43.75 MHz to 683.264 MHz see table 4 of CDCM61004 data sheet. The output frequency divider can be chosen using control pins. On PXIe-700 a 25 MHz clock input clock is used and for the output the control pins are set using 0 ohm resistors R187 – R193. The factory default settings for output clock is 125 MHz by populating R191, R192.

For any other clock output please contact Sundance DSP Inc.

Note: Please see appendix for pinouts

2.10 JTAG

A 14-pin 2mm pitch pin header is provided for connection to a Xilinx USB Programmer (using the standard ribbon cable). This allows access to the internals of the FPGA for configuration and debugging.

2.11 PXIe

The board conforms to PXIe specifications and provides a hybrid connector for PCIe and control signals.

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J2: **973028 from ERNI** backplane connector. This is used to provide PCIe signals in PXIe format.

J3: **214443 from ERNI** backplane connector. This is used to provide PXI control signals.

Note: Please see appendix for pinout.

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3 OPERATION

This section describes how to install the hardware and initialize various devices on PXIe-700 before using the host software.

3.1 Carrier/Motherboard

PXIe-700 provides 4 PCIe lanes on J2 PXI hybrid connector, so to establish this host interface a suitable PXI Express chassis conforming to the latest PXI Express specification which can accept PXI Express boards must be used.

3.2 Power Supplies

The PXIe host provides 3.3 volt and 12 volt input power. These voltages are brought to the board through the backplane connector. The module generates the following voltages:

1. 1.0v @16A (0.9v for -1C) : VCCINT, VCCBRAM
2. 1.8v @ 8A : VCCAUX, VCCAUX_IO, VCCO_1.8v
3. 1.3v @ 8A : VCC_LDO
4. 1.5v @ 8A : DDR3 Voltage
5. 3.3v @ 8A : VCCO_3.3v
6. 2.5v @ 8A : VCCO_2.5v
7. VADJ @ 8A : VADJ (Selectable 1.8, 2.5, 3.3V)
8. 1.0v @ 3A : MGTAVCC
9. 1.2v @ 3A : MGTAVTT
10. 1.8v @ 3A : MGTVCCAUX
11. 0.75v @ 3A : Vref, VTT

The power sequence is provided on page 6 in the **Xilinx Kintex-7 datasheet**.

3.3 VADJ voltage

The module can support different VADJ volatges 1.8v, 2.5v and 3.3v. The select pins can be set to generate the desired VADJ voltage.

SIGNAL	FPGA PIN
VADJ_SEL0	M19
VADJ_SEL1	P19

SEL1	SEL0	VADJ
0	0	1.8v
0	1	2.5v
1	0	N/A
1	1	3.3v

Rev 4.0 PCB only

SIGNAL	FPGA PIN
VADJ_EN	P23

VADJ_EN	Description
0	Disable
1	Enable

Table 4 - VADJ Select and Enable pins

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Note:

Rev 3.0 PCB

On power up VADJ voltage comes up as 1.8v. If a FMC module with VADJ 2.5v or 3.3v is populated then the module will receive 1.8v till the FPGA is configured with the right VADJ_SEL pins as described in the table above.

Rev 4.0 PCB

VADJ voltage is implemented as per FMC standard. On power up VADJ is 0v. After the FMC EEPROM is read the user can enable VADJ with right voltage using VADJ_SEL pins and VADJ_EN pin as described in the table above.

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3.4 FPGA Configuration

The on-board FPGA can be configured in three different ways

1. JTAG
2. FLASH

3.4.1 Configuring FPGA through JTAG

Connect J4 to a Xilinx JTAG emulator connected to a PC with Vivado 2016.2 . Start Vivado and Open hardware manager and connect to the local target. The FPGA device is detected by the software. Select the device and program it with the desired bit stream.

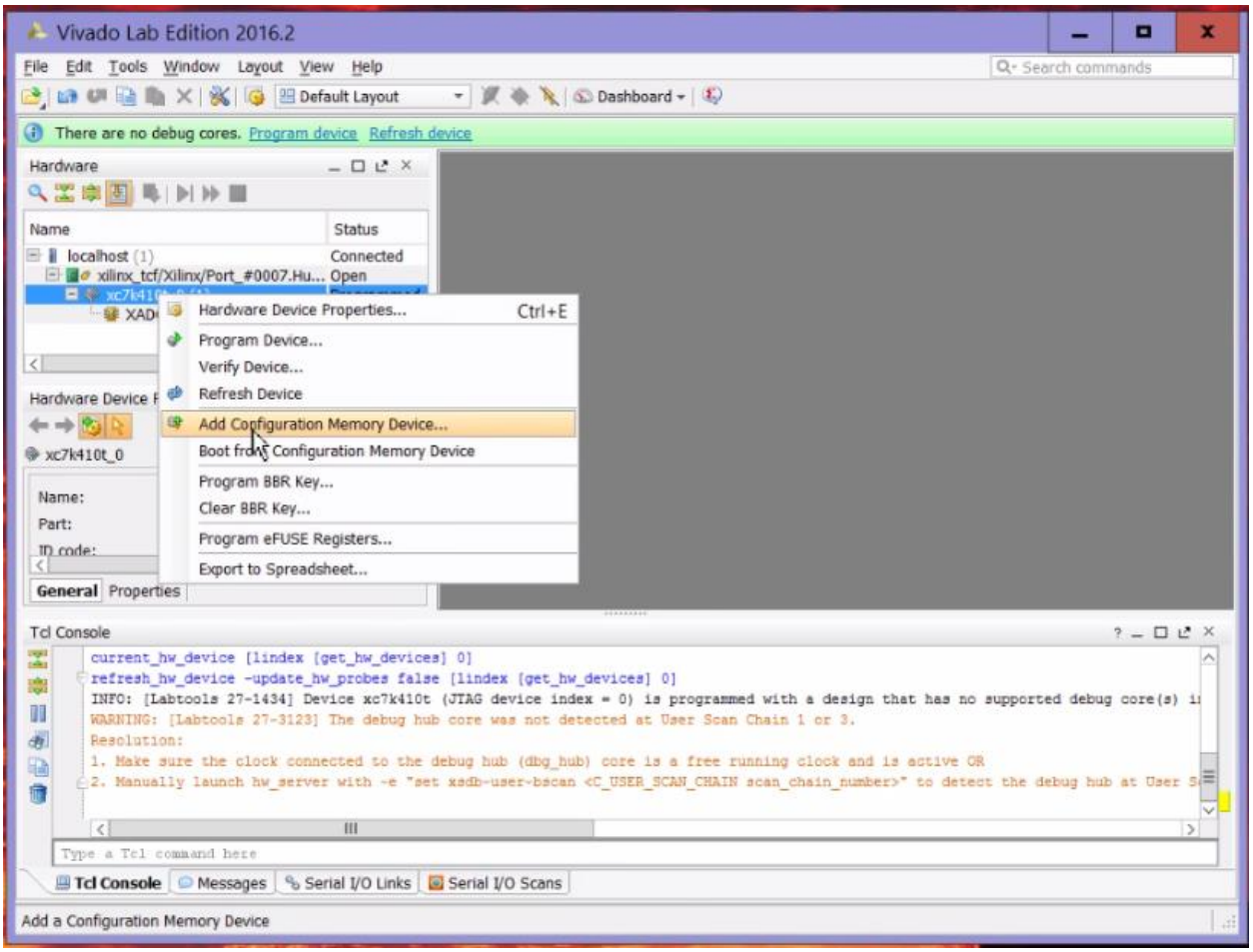

Figure 3 - JTAG Configuration

3.4.2 Configuring FPGA from Flash

The FLASH can ONLY be programmed via JTAG connection and not through the host interface. In order to program the flash, connect to the FPGA via JTAG. Right click on FPGA -> Add configuration memory device as shown above. Select PC28F00AP30T x16 BPI as your flash device and use .mcs and .prm files to burn the flash.

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Once the flash has been programmed set switch SW1 to Master BPI mode.

Note: Set pins 3 to 5 on switch SW1 to OFF, ON, OFF for the FPGA to boot from flash.

Multiple bitstreams can be stored in the flash by setting the Warm Boot Start Address (WBSTAR) register available in 7-series FPGA. More information is available in the reconfiguration and multiboot section in 7 series FPGAs configuration user guide UG470

https://www.xilinx.com/support/documentation/user_guides/ug470_7Series_Config.pdf

Note: The multi-boot feature has not been tested as of now. Please refer to the above link.

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4 APPLICATION DEVELOPMENT

The board comes with a demonstration, confidence-test package called SCom-AXI-BSP.zip. The BSP (Board Support Package) will include drivers for Windows (Linux OS is optional), Host API and application program. The host API is based on Sundance Scom (Sundance Communication) library along with a default FPGA bitstream which will provide users a multi-channel DMA interface to talk to the user application. The default package is not suitable for developing user application and is simply for confidence building. If a complete driver and host API with the relevant IP cores and libraries is required, please contact SDSP sales team for pricing and delivery.

The document section has all the instructions for installation, setup and testing the hardware. Please read the documents carefully for proper functionality. For support please contact Sundance DSP on the support forum **https://www.sundancedsp.com/forum/** or write to support@sundancedsp.com

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APPENDIX

4.1 Pinout

4.1.1 PXIe

This board conforms to PXIe specification.

J2: **973028 from ERNI** backplane connector. This is used to provide PCIe signals from PXIe host to the board.

Note: The control signals are connected to 1.8v Bank (LVCMOS_18). All the differential signals are LVDS signals.

PIN	A	FPGA_PIN Rev 3.0	FPGA_PIN Rev 4.0	B	FPGA_PIN Rev 3.0	FPGA_PIN Rev 4.0	C
1	PXIe_CLK+	AD18	AD18	PXIe_CLK-	AE18	AE18	GND
2	PRSNT#			PWREN			GND
3	SMBDAT	M29	M29	SMBCLK	M28	M28	GND
4	MPWRGD			PERST#	AH19	AH19	GND
5	1PETP0	Y2	Y2	1PETN0	Y1	Y1	GND
6	1PETP2	U4	U4	1PETN2	U3	U3	GND
7	1PETP3	T2	T2	1PETN3	T1	T1	GND
8	1PETP5			1PETN5			GND
9	1PETP6			1PETN6			GND
10	RSV			RSV			GND

PIN	D	FPGA_PIN Rev 3.0	FPGA_PIN Rev 4.0	E	FPGA_PIN Rev 3.0	FPGA_PIN Rev 4.0	F
1	PXIe_SYNC+	AF17	AD17	PXIe_SYNC-	AG17	AD16	GND
2	PXIe_DSTARB+	AH17	AH17	PXIe_DSTARB-	AJ17	AJ17	GND
3	RSV			RSV			GND
4	RSV			RSV			GND
5	1PERP0	AA4	AA4	1PERN0	AA3	AA3	GND
6	1PERP2	W4	W4	1PERN2	W3	W3	GND
7	1PERP3	V6	V6	1PERN3	V5	V5	GND
8	1PERP5			1PERN5			GND
9	1PERP6			1PERN6			GND
10	RSV			RSV			GND

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PIN	G	FPGA_PIN Rev 3.0	FPGA_PIN Rev 4.0	H	FPGA_PIN Rev 3.0	FPGA_PIN Rev 4.0	I
1	PXIe_DSTARC+	AF15	AF15	PXIe_DSTARC-	AG14	AG14	GND
2	PXIe_DSTARA+	AJ19	AF17	PXIe_DSTARA-	AK19	AG17	GND
3	RSV			RSV			GND
4	1REFCLK+	U8	U8	1REFCLK-	U7	U7	GND
5	1PETP1	V2	V2	1PETN1	V1	V1	GND
6	1PERP1	Y6	Y6	1PERN1	Y5	Y5	GND
7	1PETP4			1PETN4			GND
8	1PERP4			1PERN4			GND
9	1PETP7			1PETN7			GND
10	1PERP7			1PERN7			GND

Table 5 - PXIe-700 J2 Pinout

J3: **214443 from ERNI** backplane connector. This is used to provide PXI control signals.

Note: These signals are connected to 1.8v Bank

PIN	A	FPGA_PIN	B	FPGA_PIN	C	FPGA_PIN
1	GA4	AB17	GA3	AC19	GA2	AB19
2	5v_AUX		GND		SYS_EN	
3	12v		12V		GND	
4	GND		GND		3.3V	
5	PXI_TRIG3	AB15	PXI_TRIG4	AC16	PXI_TRIG5	AC15
6	PXI_TRIG2	AA15	GND		ATNLED	Y16
7	PXI_TRIG1	AE15	PXI_TRIG0	AC17	ATNSW#	AA16
8	RSV		GND		RSV	

PIN	D	FPGA_PIN	E	FPGA_PIN	F	FPGA_PIN
1	GA1	AB18	GA0	AA18		
2	WAKE		ALERT#	AG19		
3	GND		GND		GND	
4	3.3V		3.3V		GND	
5	GND		PXI_TRIG6	AC14	GND	
6	PXI_STAR	AA17	PXI_CLK10	AF18	GND	
7	GND		PXI_TRIG7	AD14		
8	PXI_LBL6	AK18	PXI_LBR6	AJ18		

Table 6 - PXIe-700 J2 pinout

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4.1.2 HPC FMC

PXIe_700 FMC HPC Pinout (J1 Connector)										
S.No	Row A	FPGA Pin	Row B	FPGA Pin	Row C	FPGA Pin	Row D	FPGA Pin	Row E	FPGA Pin
1	GND		NC		GND		FMC_PG_C2M	H29	GND	
2	FMC_M2C_DP1+	H6	GND		FMC_C2M_DP0+	K2	GND		FMC_CC_HA01+	H14
3	FMC_M2C_DP1-	H5	GND		FMC_C2M_DP0-	K1	GND		FMC_CC_HA01-	G14
4	GND		FMC_M2C_DP9+	P6	GND		FMC_M2C_GBTCLK0+	G8	GND	
5	GND		FMC_M2C_DP9-	P5	GND		FMC_M2C_GBTCLK0-	G7	GND	
6	FMC_M2C_DP2+	G4	GND		FMC_M2C_DP0+	K6	GND		FMC_HA05+	L16
7	FMC_M2C_DP2-	G3	GND		FMC_M2C_DP0-	K5	GND		FMC_HA05-	K16
8	GND		FMC_M2C_DP8+	M6	GND		FMC_CC_LA01+	D26	GND	
9	GND		FMC_M2C_DP8-	M5	GND		FMC_CC_LA01-	C26	FMC_HA09+	L15
10	FMC_M2C_DP3+	F6	GND		FMC_LA06+	H30	GND		FMC_HA09-	K15
11	FMC_M2C_DP3-	F5	GND		FMC_LA06-	G30	FMC_LA05+	G29	GND	
12	GND		FMC_M2C_DP7+	A8	GND		FMC_LA05-	F30	FMC_HA13+	K14
13	GND		FMC_M2C_DP7-	A7	GND		GND		FMC_HA13-	J14
14	FMC_M2C_DP4+	E4	GND		FMC_LA10+	D29	FMC_LA09+	B30	GND	
15	FMC_M2C_DP4-	E3	GND		FMC_LA10-	C30	FMC_LA09-	A30	FMC_HA16+	L12
16	GND		FMC_M2C_DP6+	B6	GND		GND		FMC_HA16-	L13
17	GND		FMC_M2C_DP6-	B5	GND		FMC_LA13+	B28	GND	
18	FMC_M2C_DP5+	D6	GND		FMC_LA14+	A25	FMC_LA13-	A28	FMC_HA20+	H11
19	FMC_M2C_DP5-	D5	GND		FMC_LA14-	A26	GND		FMC_HA20-	H12
20	GND		FMC_M2C_GBTCLK1+	J8	GND		FMC_CC_LA17+	F21	GND	
21	GND		FMC_M2C_GBTCLK1-	J7	GND		FMC_CC_LA17-	E21	FMC_HB03+	J19
22	FMC_C2M_DP1+	J4	GND		FMC_CC_LA18+	F20	GND		FMC_HB03-	H19
23	FMC_C2M_DP1-	J3	GND		FMC_CC_LA18-	E20	FMC_LA23+	B22	GND	
24	GND		FMC_C2M_DP9+	M2	GND		FMC_LA23-	A22	FMC_HB05+	K19
25	GND		FMC_C2M_DP9-	M1	GND		GND		FMC_HB05-	K20
26	FMC_C2M_DP2+	H2	GND		FMC_LA27+	C19	FMC_LA26+	B18	GND	
27	FMC_C2M_DP2-	H1	GND		FMC_LA27-	B19	FMC_LA26-	A18	FMC_HB09+	F26
28	GND		FMC_C2M_DP8+	L4	GND		GND		FMC_HB09-	E26
29	GND		FMC_C2M_DP8-	L3	GND		FMC_TCK_BUF		GND	
30	FMC_C2M_DP3+	F2	GND		FMC_I2C_SCL		FMC_TDI_BUF		FMC_HB13+	G12
31	FMC_C2M_DP3-	F1	GND		FMC_I2C_SDA		FMC_TDO_BUF		FMC_HB13-	F16
32	GND		FMC_C2M_DP7+	A4	GND		V3P3		GND	
33	GND		FMC_C2M_DP7-	A3	GND		FMC_TMS_BUF		NC	
34	FMC_C2M_DP4+	D2	GND		GND		NC		NC	
35	FMC_C2M_DP4-	D1	GND		V12P0		GND		GND	
36	GND		FMC_C2M_DP6+	B2	GND		V3P3		NC	
37	GND		FMC_C2M_DP6-	B1	V12P0		GND		NC	
38	FMC_C2M_DP5+	C4	GND		GND		V3P3		GND	
39	FMC_C2M_DP5-	C3	GND		V3P3		GND		VADJ	
40	GND		NC		GND		V3P3		GND	

PXIe_700 FMC HPC Pinout (J1 Connector) Cont.....										
S.No	Row F	FPGA Pin	Row G	FPGA Pin	Row H	FPGA Pin	Row J	FPGA Pin	Row K	FPGA Pin
1	FMC_PG_M2C	J29	GND		VREF_A_M2C	G24	GND		NC	
2	GND		FMC_M2C_CLK1+	D17	FMC_PRSNT_M2C_B	M20	NC		GND	
3	GND		FMC_M2C_CLK1-	D18	GND		NC		GND	
4	FMC_CC_HA00+	G13	GND		FMC_M2C_CLK0+	D27	GND		NC	
5	FMC_CC_HA00-	F13	GND		FMC_M2C_CLK0-	C27	GND		NC	
6	GND		FMC_CC_LA00+	C25	GND		FMC_HA03+	F15	GND	
7	FMC_HA04+	J16	FMC_CC_LA00-	B25	FMC_LA02+	E29	FMC_HA03-	E16	FMC_HA02+	E14
8	FMC_HA04-	H16	GND		FMC_LA02-	E30	GND		FMC_HA02-	E15
9	GND		FMC_LA03+	C29	GND		FMC_HA07+	D12	GND	
10	FMC_HA08+	H15	FMC_LA03-	B29	FMC_LA04+	E28	FMC_HA07-	D13	FMC_HA06+	C15
11	FMC_HA08-	G15	GND		FMC_LA04-	D28	GND		FMC_HA06-	B15
12	GND		FMC_LA08+	G28	GND		FMC_HA11+	D14	GND	
13	FMC_HA12+	K13	FMC_LA08-	F28	FMC_LA07+	B27	FMC_HA11-	C14	FMC_HA10+	B14
14	FMC_HA12-	J13	GND		FMC_LA07-	A27	GND		FMC_HA10-	A15
15	GND		FMC_LA12+	C24	GND		FMC_HA14+	B13	GND	
16	FMC_HA15+	J11	FMC_LA12-	B24	FMC_LA11+	G27	FMC_HA14-	A13	FMC_CC_HA17+	F12
17	FMC_HA15-	J12	GND		FMC_LA11-	F27	GND		FMC_CC_HA17-	E13
18	GND		FMC_LA16+	H26	GND		FMC_HA18+	C12	GND	
19	FMC_HA19+	L11	FMC_LA16-	H27	FMC_LA15+	F25	FMC_HA18-	B12	FMC_HA21+	A11
20	FMC_HA19-	K11	GND		FMC_LA15+	E25	GND		FMC_HA21-	A12
21	GND		FMC_LA20+	D22	GND		FMC_HA22+	D11	GND	
22	FMC_HB02+	J17	FMC_LA20-	C22	FMC_LA19+	A20	FMC_HA22-	C11	FMC_HA23+	F11
23	FMC_HB02-	H17	GND		FMC_LA19-	A21	GND		FMC_HA23-	E11
24	GND		FMC_LA22+	C20	GND		FMC_HB01+	H20	GND	
25	FMC_HB04+	L17	FMC_LA22-	B20	FMC_LA21+	D21	FMC_HB01-	G20	FMC_HB00+	K18
26	FMC_HB04-	L18	GND		FMC_LA21-	C21	GND		FMC_HB00-	J18
27	GND		FMC_LA25+	A16	GND		FMC_HB07+	E23	GND	
28	FMC_HB08+	E24	FMC_LA25-	A17	FMC_LA24+	C17	FMC_HB07-	D23	FMC_HB06+	B23
29	FMC_HB08-	D24	GND		FMC_LA24-	B17	GND		FMC_HB06-	A23
30	GND		FMC_LA29+	D16	GND		FMC_HB11+	G23	GND	
31	FMC_HB12+	G19	FMC_LA29-	C16	FMC_LA28+	E19	FMC_HB11-	H24	FMC_HB10+	F23
32	FMC_HB12-	E18	GND		FMC_LA28-	D19	GND		FMC_HB10-	G25
33	GND		FMC_LA31+	G18	GND		NC		GND	
34	NC		FMC_LA31-	F18	FMC_LA30+	G17	NC		NC	
35	NC		GND		FMC_LA30-	F17	GND		NC	
36	GND		FMC_LA33+	G22	GND		NC		GND	
37	NC		FMC_LA33-	F22	FMC_LA32+	H21	NC		NC	
38	NC		GND		FMC_LA32-	H22	GND		NC	
39	GND		VADJ		GND		NC		GND	
40	VADJ		GND		VADJ		GND		NC	

Table 7 - HPC FMC Pinout

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4.1.3 SFP+

Note: The control signals are connected to 1.8v bank

PXIe 700 SFP+ Pinout		
S.No	**SFP+ Pin**	**FPGA Pin**
1	SFP_TX+	P2
2	SFP_TX-	P1
3	SFP_RX+	T6
4	SFP_RX-	T5
5	SFP_TX_FAULT	AH16
6	SFP_TX_DISABLE	AJ16
7	SFP_MOD_DETECT	AE16
8	SFP_RS0	Y18
9	SFP_RS1	Y19
10	SFP_LOS	AF16

Table 8 - SFP+ Pinout

4.1.4 MMCX

PXIe 700 MMCX Pinout		
Connector	**Pin_name**	**FPGA Pin**
P1	MGTX_REFCLK+	N8
P2	MGTX_REFCLK-	N7
P3	FPGA_REFCLK+	U28
P4	FPGA_REFCLK-	U27
P5	MGTX_AUX_TX+	N4
P6	MGTX_AUX_TX-	N3
P7	MGTX_AUX_RX+	R4
P8	MGTX_AUX_RX-	R3

Table 9 - MMCX Pinout

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4.1.5 LEDS

Note: Pins are connected to 2.5v bank

PXIe 700 LED Pinout		
S.No	**LED**	**FPGA Pin**
1	D2	H29
2	D3	L26
3	D4	L27
4	D5	M27
5	D6	N27

Table 10 - LEDs Pinout

4.1.6 Clocks

Note: Pins are connected to 2.5v bank

PXIe 700 Clock Pinout			
S.No	**Pin_name**	**FPGA Pin**	**Clock Frequency**
1	FPGA_EMCCLK	R24	66 MHz
2	FPGA_VCXO_CLK	L25	20 MHz
3	MGT_SYS_CLK0+	C8	125 MHz
4	MGT_SYS_CLK0-	C7	125 MHz
5	MGT_SYS_CLK1+	L8	125 MHz
6	MGT_SYS_CLK1-	L7	125 MHz
7	FPGA_SYS_CLK+	K28	125 MHz
8	FPGA_SYS_CLK-	K29	125 MHz

Table 11 - Clocks pinout

4.1.7 DDR3 Interface

PXIe_700 DDR3 Pinout Bank 1			
Signal	**FPGA Pin**	**Signal**	**FPGA Pin**
A0	AD8	CLK+	AB9
A1	AC10	CLK-	AC9
A2	AB10	DQ0	AD3
A3	AB13	DQ1	AC2
A4	AA13	DQ2	AC1
A5	AA10	DQ3	AC5
A6	AA1	DQ4	AC4
A7	Y10	DQ5	AD6
A8	Y11	DQ6	AE6

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A9	AB8	DQ7	AC7
A10	AA8	DQ8	AF2
A11	AB12	DQ9	AE1
A12	AA12	DQ10	AF1
BA0	AC11	DQ11	AE4
BA1	AC12	DQ12	AE3
BA2	AE8	DQ13	AE5
RAS#	AD9	DQ14	AF5
CAS#	AE9	DQ15	AF6
WE#	AE11	DQ16	AJ4
CS#	AF11	DQ17	AH6
RESET#	AD12	DQ18	AH5
CKE	AD11	DQ19	AH2
ODT	AG10	DQ20	AJ2
DM0	AD4	DQ21	AJ1
DM1	AF3	DQ22	AK1
DM2	AH4	DQ23	AJ3
DM3	AF8	DQ24	AF7
DQS0+	AD2	DQ25	AG7
DQS0-	AD1	DQ26	AJ6
DQS1+	AG4	DQ27	AK6
DQS1-	AG3	DQ28	AJ8
DQS2+	AG2	DQ29	AK8
DQS2-	AH1	DQ30	AK5
DQS3+	AH7	DQ31	AK4
DQS3-	AJ7		

PXIe_700 DDR3 Pinout Bank 2			
Signal	**FPGA Pin**	**Signal**	**FPGA Pin**
A0	AC22	CLK+	AB22
A1	AC25	CLK-	AB23
A2	AB24	DQ0	AA26
A3	AB20	DQ1	W27
A4	AA20	DQ2	W28
A5	AC21	DQ3	W29
A6	AC20	DQ4	Y29
A7	AA23	DQ5	AA27
A8	AA22	DQ6	AB28
A9	AA21	DQ7	AA25
A10	Y21	DQ8	AC30

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A11	Y24	DQ9	Y30
A12	Y23	DQ10	AA30
BA0	AD24	DQ11	AB29
BA1	AC24	DQ12	AB30
BA2	AD22	DQ13	AD27
RAS#	AD21	DQ14	AD28
CAS#	AE21	DQ15	AB27
WE#	AE23	DQ16	AH29
CS#	AF23	DQ17	AE28
RESET#	AD23	DQ18	AF28
CKE	AE24	DQ19	AE30
ODT	AF22	DQ20	AF30
DM0	Y26	DQ21	AJ28
DM1	AC29	DQ22	AJ29
DM2	AG29	DQ23	AG30
DM3	AC26	DQ24	AJ27
DQS0+	Y28	DQ25	AK28
DQS0-	AA28	DQ26	AH26
DQS1+	AD29	DQ27	AH27
DQS1-	AE29	DQ28	AF26
DQS2+	AK29	DQ29	AF27
DQS2-	AK30	DQ30	AJ26
DQS3+	AG27	DQ31	AK26
DQS3-	AG28		

Table 12 - DDR3 Pinout

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4.1.8 J5 Header

Note: Pins are connected to 2.5v bank

J5 Header Pinout		
Pin No	**Signal**	**FPGA Pin**
1	V2P5	-
2	GPIO_0	R28
3	GPIO_1	T28
4	GPIO_2	T26
5	GPIO_3	T27
6	GPIO_4	T25
7	GPIO_5	U25
8	GPIO_6	U30
9	GPIO_7	V26
10	GND	-

Table 13 - J5 Header Pinout

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