NES-IPCORE1553
MIL-STD1553 IP CORE Bus Controller,Remote Terminal and Monitoring

// OVERVIEW

Mil-Std-1553 Intellectual Property for FPGAs and ASIC

Suitable for any MIL-STD-1553 BC, RT, MT implementation

Compatible to Enhanced DDC Mini-Ace* interface and functionality, works with existing software drivers

Eliminates risks related to parts obsolescence

Small FPGA area utilization

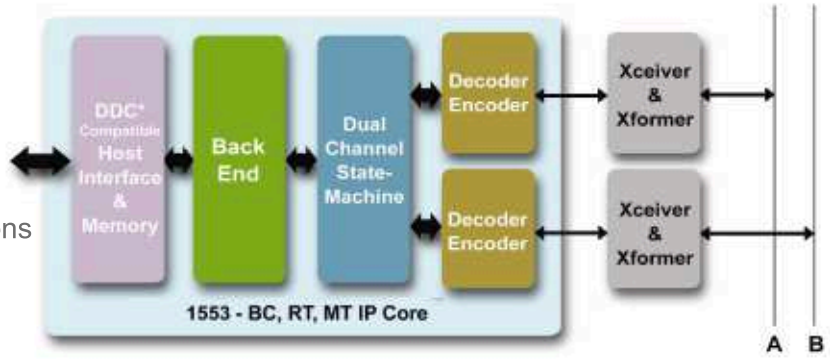
Supports any even clock frequency

Modular architecture allowing flexible implementations

Provided with full verification environment

Passed full RT validation testing by 3rd party

Based on vendor and technology independent VHDL code



// HIGHLIGHTS

Designed from ground up for use in aerospace, avionics and military MIL-STD-1553 solutions, The MIL-STD-1553 IP products,offer uniquely compact, robust and reliable BC, RT, MT solutions for any PLD/FPGA and ASIC device. They were developed following the company's unflagging commitment to quality and excellence along with strict adherence to meeting the stringent requirements of the military and aerospace specifications.

A Core For Any Mil-Std-1553 Implementation

The NES-IPCORE1553 is suitable for any Mil-Std-1553 implementation. The core incorporates a backend logic that arranges the messages in a predefined memory structure, which simplifies the interface between the 1553 bus and the local CPU. The NES-IPCORE1553 core can act as a full replacement (2nd source) for DDC enhanced mini-Ace* devices as the data is arranged in the same way.

Small Gate Count

The NES-IPCORE1553 requires very small space from FPGA for complex applications.

The following table shows examples of the area usage, in different FPGA devices:

Vendor	Product Family	Area Usage (4-LUT count)	
		BC+RT+MT	RT Only
Altera	Stratix	3326	2257
	Cyclone	3330	2261
Xilinx	Virtex-II	3020	2066
	Spartan 3	3017	2063

These numbers are approximate. Other FPGA vendors and families are available
Actual area usage may vary according to core configuration.

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// SPECIFICATIONS

Backend Interface
Includes DDC's Enhanced mini ACE* interface, compatible with existing drivers and applications.
No need to rewrite drivers' code and eliminates replacement risk

3rd Party Validation
The NES-IPCORE1553 successfully passed the full MIL-STD-1553B Notice 2 RT Validation test, according to a test plan from MIL-HDBK-1553A. Validation tests were performed by an independent 3rd party laboratory.

Manchester Decoder
The unique Manchester decoder can work with any even clock frequency from 12Mhz and up to reduce clock sources and clock domains on board (reduces EMI/RFI). Advanced algorithms for filtering out noise and disturbances enable the core to operate in harsh environments.

Advanced Verification
To ensure a fully reliable and robust product the core was developed using an advanced verification environment that includes a Random-Generation engine,Code-Coverage and assertion tools. All MIL-STD-1553B functions and performance requirements were verified.

Simple Integration
In order to simplify the integration of the core, a sample VHDL design that uses the core is provided, including:
- A comprehensive user's manual.
- A VHDL gate level model of the core for the target technology.
- A Transceiver VHDL model that connects the core with 2 buses.
- A bus tester VHDL model that generates 1553 messages and checks the return replies.
- A top Test bench that instantiates all of these components to a working example.
- A simulation script for compiling and running the core.

Compatibility
- MIL-STD-1553B Notice 2
- RT Validated according to test plan from MIL-HDBK-1553A
- 1Mbps Data Rate
- Connects to any transceiver-transformer pair
- Enhanced DDC Mini-Ace interface

RAM
- 2, 4, 8, 16, 32, 64K by 16 bits
- Limited by FPGA resources only

FPGA Requirements
- 10 pins to connect to transceiver
- Standard FPGA pads
- Internal FPGA Dual Port RAM of 2K x 16 or higher.

Clock
- Any even frequency from 12MHz and up

Supported FPGAs
Any FPGA with sufficient number of LUTs and memory and FPGA families from the following vendors : Xilinx,Actel, Altera, Lattice, QuickLogic

Available Configurations
NES-IPCORE1553-BCRTMT: Bus Controller + Remote Terminal + Monitor Terminal
NES-IPCORE1553-RT: Remote Terminal only