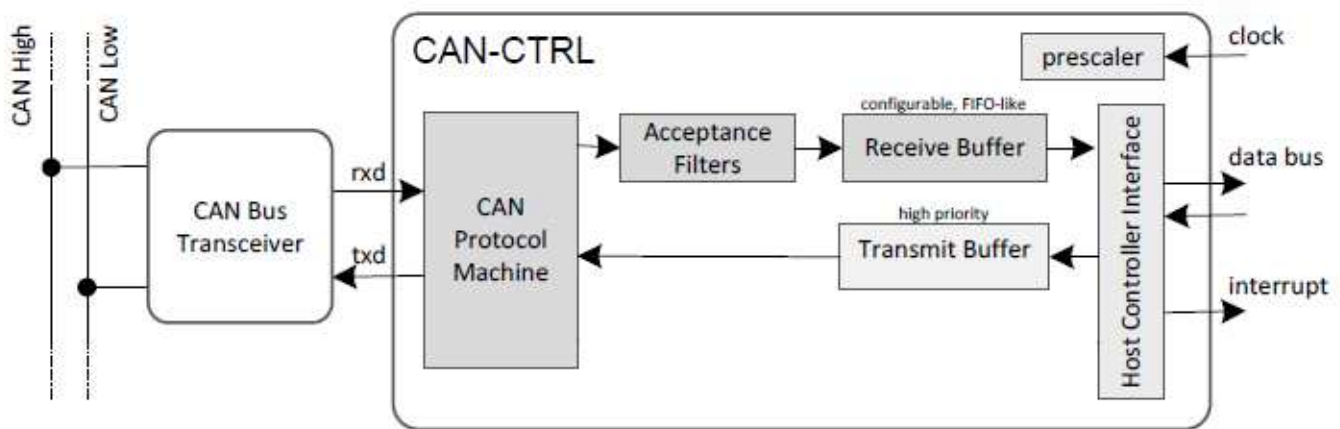


// OVERVIEW



CAN Specification 2.0B

Standard and Extended Data and Remote Frames

Enhanced Functionality

Error Analysis features enabling diagnostics,
system maintenance and system optimization

Last error type capture, Arbitration lost position capture

Programmable Error Warning Limit

Listen-Only Mode enables CAN bus traffic analysis
and automatic bit-rate detection

Flexible Message Buffering and Filtering, Configurable number of receive buffers, 2 to 31

One high-priority transmit buffer

Configurable number of lower-priority transmit buffers, 0 to 16

Configurable number of independently programmable

29-bit acceptance filters, 1 to 16

Programmable data rate up to 1 Mbit/s, Programmable baud rate prescaler. 1/2 up to 1/256

Single Shot Transmission Mode for lower software overhead
and fast reloading of transmit buffer

Flexible programmable interrupt sources

Generic 8-bit host-controller interface

Buffers can be implemented as Flip-Flops or RAM

// FUNCTIONAL DESCRIPTION

Implements a CAN protocol bus controller that performs serial communication according to the CAN 2.0A and 2.0B specifications. The CAN protocol uses a multi-master bus configuration for the transfer of frames between nodes of the network and manages error handling with no burden on the host processor. The NES-IP CORE-CAN enables the user to set up economic and reliable links between various components. It appears as a memory-mapped I/O device to the host processor, which accesses the CAN megafunction to control the transmission or reception of frames.

The NES-IP CORE-CAN is easy to use and integrate, featuring programmable interrupts, data and baud rates; a configurable number of independently programmable acceptance filters; and a generic processor interface. It implements a flexible buffering scheme, allowing fine-tuning of the megafunction size to the requirements of each specific application. The number of receive buffers is synthesis-time configurable from 2 to 31. Two types of transmit buffers are implemented: a high-priority primary transmit buffer (PTB) and a lower-priority secondary transmit buffer (STB). The PTB can store one message, while the number of included buffer slots for the STB is synthesis-time configurable 0 to 16 slots. Moreover, an optional wrapper instantiating multiple CAN controllers eases integration in cases where multiple bus-nodes need to be controlled by the same host processor.

The NES-IP CORE-CAN is robustly verified and proven in multiple production designs.

Functional Description

The NES-IP CORE-CAN is founded on the basic CAN principle and meets all constraints of the CAN-specification 2.0B. Several 13-byte buffers are used for buffering received or transmitted messages. The number of buffers can be selected before synthesis. Selecting a large number of buffers disables the need for real-time reaction to CAN messages for the host processor, which significantly eases software development of the system application.

The included high-priority transmit buffer can be used to transmit an important message as fast as possible, even if several lower-priority messages are pending for transmission.

The host interface contains all necessary registers for controlling and configuring the NES-IP CORE-CAN. The host is able to read and write all registers as a conventional RAM in memory mapped mode. The interface to the host is software configurable. All events on the CAN data bus or in the CAN controller NES-IP CORE-CAN are signaled using an interrupt. Every interrupt source may be individually enabled or disabled. The NES-IP CORE-CAN controller contains up to sixteen software-programmable 29-bit acceptance filters that can be used to block unwanted CAN messages, which reduces the load to the host controller.

The host controller interface is connected with the memory module by an 8-bit data and a 6-bit address bus. This enables easy interfacing to many host controller types, and therefore, quick integration with a microcontroller

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