Unit / Module Description:	Dual ADC/DAC FMC
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Original Author:	G K Parker

FMC Mezzanine

(ADC/DAC)

SMT-FMC311

Sundance Multiprocessor Technology Ltd, Chiltern House,
Waterside, Chesham, Bucks. HP5 1PS.

Revision History

Issue	Changes Made	Date	Initials
1.0	First release as SMT-FMC311. Based upon SMT-FMC-GSI.	25/9/15	GKP
1.1	Added specification details for clock and trigger inputs	06Oct15	SEC
1.2	Revised and detailed FPGA pin allocation and FPGA configuration, added eeprom detail, other minor corrections	22Oct15	SEC

Table of Contents

1 Introduction

This document describes the hardware features and some operational details.

Some discussion is made of how these features can be implemented with specific devices.

1.1 Main Features

1.1.1 Hardware

This board consists of the following major hardware features:

1) VITA57.1 FMC-LPC™ (subset, no MGT) mezzanine.
2) One dual channel ADC.
3) One dual channel DAC.
4) PLL clock synthesizer.
5) External clock and trigger inputs.

2 Notes

Several part numbers are described in the text. With the exception of the ADC and DAC, these are possible part numbers, and alternative devices may be designed in at a later date but the performance/specification will not alter.

2.1 Abbreviations / Definitions

ADC	Analog to Digital Converter.
FPGA	Field Programmable Gate Array.
GPIO	General Purpose Input Output.
I^2C	Inter-integrated Circuit. A two wire low speed serial interface.
RAM	Random Access Memory.

2.2 History and benefits of the VITA 57.1 FMC Module Standard

The original TIM Module was designed in the early 1990's to be used with the TMS320C40 Digital Signal Processor to build scalable Multiprocessor System Solutions and Embedded Systems. It was never intended to be populated with FPGAs, nor was it designed to be a Data Acquisition Module. Many companies, among them Sundance, did produce data acquisition TIMs, but it was always necessary to use cables to route analog/digital signals to the outside World.

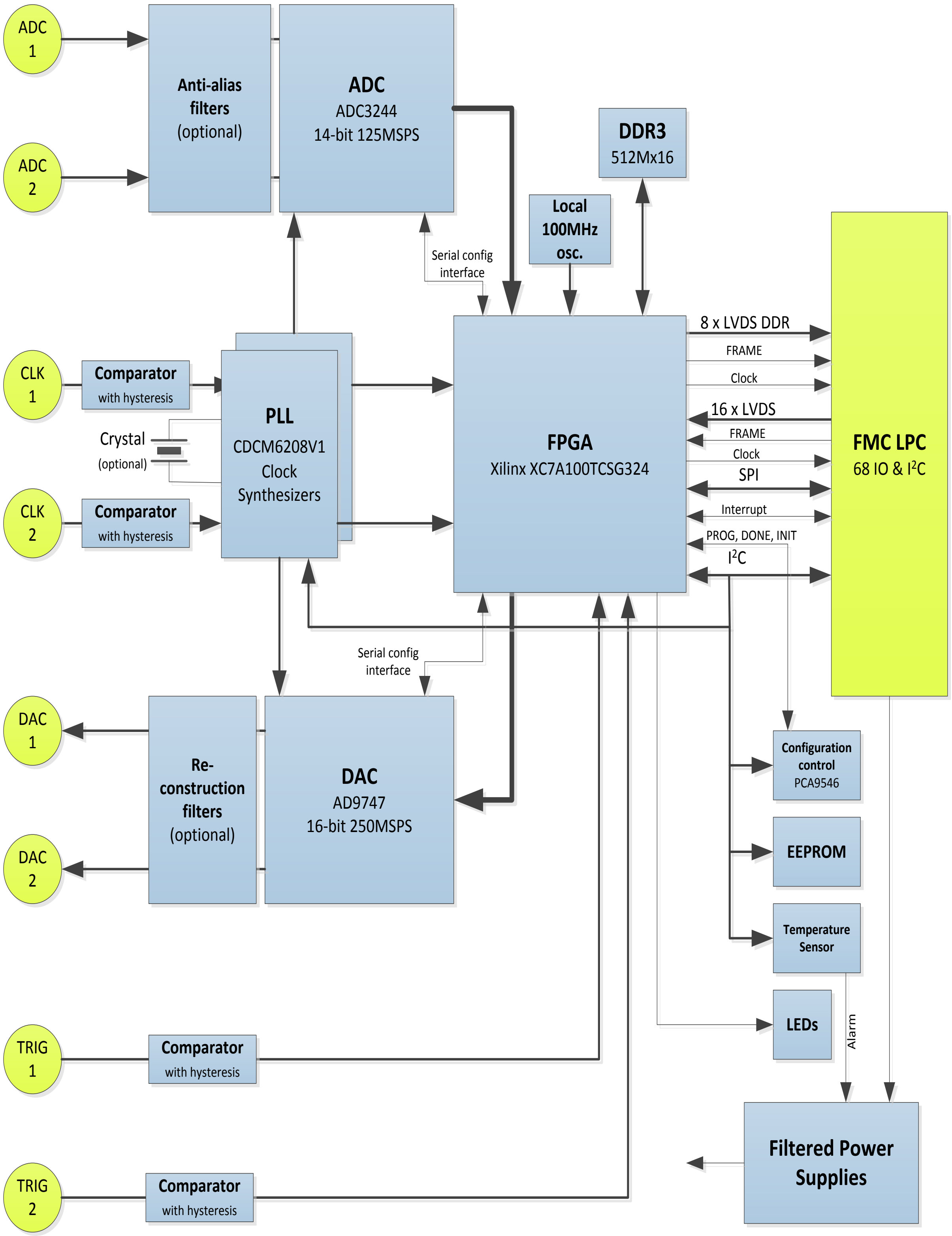
In the late 2000's, the idea of making a dedicated FPGA Mezzanine Card was proposed. It was eventually adopted as a VSO standard, called VITA57.1 (specifications are $100.00 and can be bought from VITA [3]).

The target application for FMC are cards that can be plugged into an FPGA-based system to make a DAQ solution. It has the high-pin connectors at one end of the PCB card and the analog signal connectors on the opposite end, thereby eliminating the requirement for any internal cables from a Module to an external case. The FMC's connectors are parallel to the housing and allows the smallest possible trace-length between high-speed ADC/DAC semiconductors and the cables required to connect RF units.

The prime market for FMC is ruggedized applications and extreme care has been taken with the heat-dissipation requirements and provision of effective ways to take heat away from the card. Today standardized aluminium cooling enclosures can be bought from a range of sources. See paragraph 6 below.   The enclosure is also part of the EMC-shielding of the analog circuits, hence solving multiple problems.

3 Block Diagram

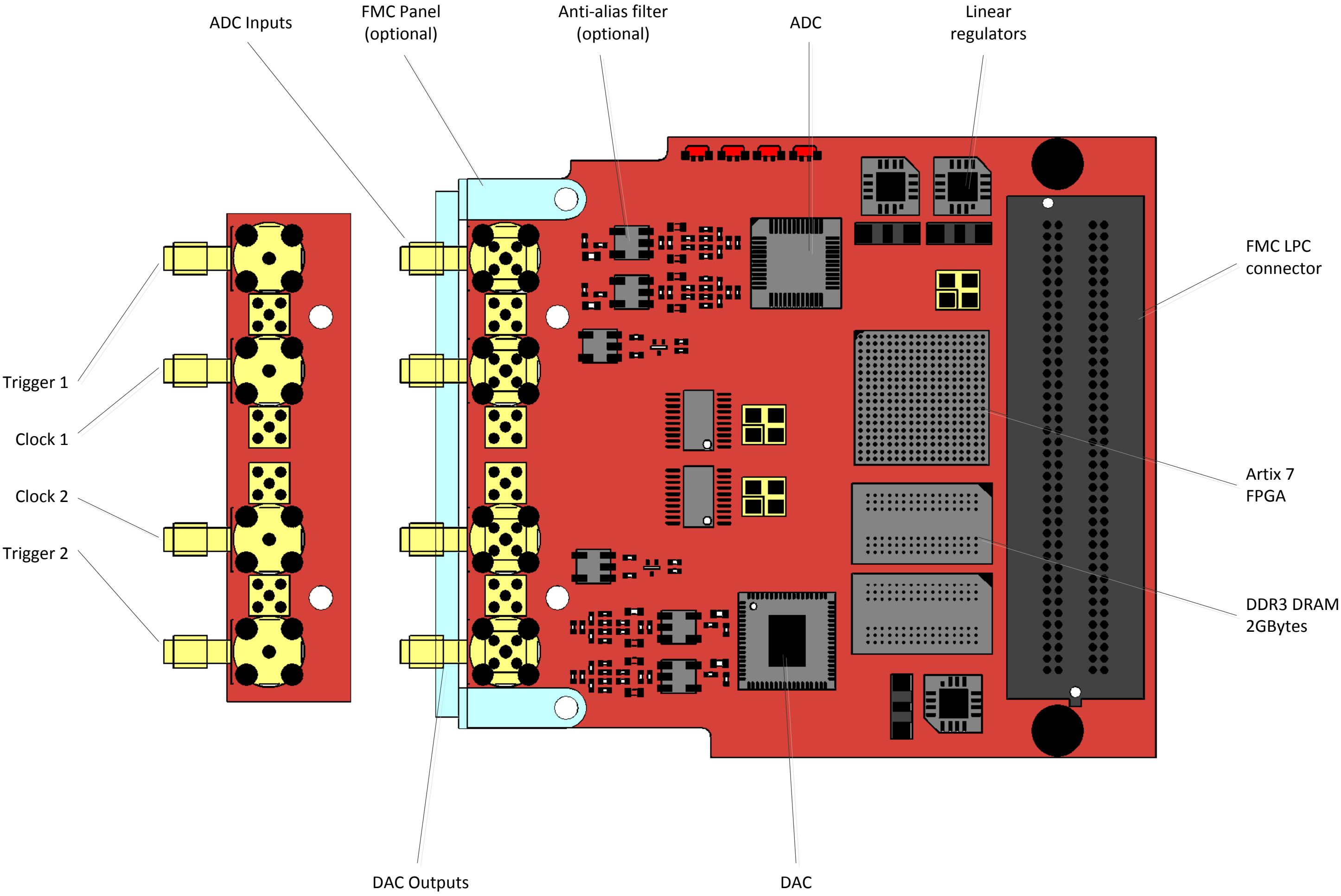
Below is the block diagram of the SMT-FMC311:



4 PCB Layout

The SMT-FMC311 is an FMC mezzanine with an LPC connector. The major component placement is shown here.

Component side view



5 Electronic Design

5.1 ADC

The module includes a single TI ADC3244 [4] device.

This is a dual 14-bit ADC able to sample from 15 up to 125MSPS. It has a maximum power dissipation of 325mW (typically 233mW). SNR is typically around 72dBFS and SFDR around 90dBc.

The data interface to the FPGA is by means of two DDR LVDS pairs (per channel). This data is clocked into the FPGA by the ADC signal Bit_Clock, which is derived from the synthesiser clock to the ADC.

The ADC's internal registers are configured over a 4-wire serial interface from the FPGA.

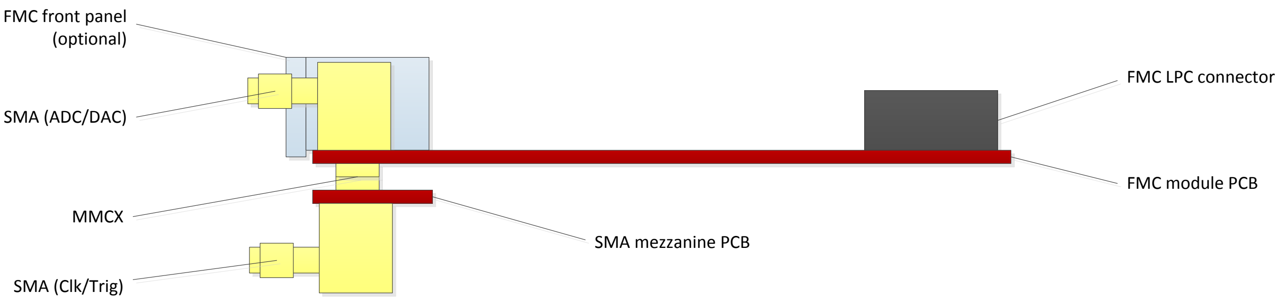
A total of 18 FPGA I/O pins are required with a bank voltage of 1.8V. See the FPGA pin allocation below for details.

The analog inputs are DC coupled and driven to the ADC via single-ended to differential op-amps. The input range for full scale is 2.2Vpp, with an impedance of 50Ω. Bandwidth is 50MHz (1dB). Absolute maximum input amplitude is 20dBm (min.).

Anti-alias filter options include:

- An on-board 4th order (24dB/octave) low pass filter constructed using 2 op-amp stages (single device package).
- A custom surface mount module replacing the input stage components.
- An externally connected unit, e.g. Mini-Circuits (as an example) produce many suitable in-line filters with differing responses. For example, the BLP-21.4-75+ has a -3dB point at 24.5MHz and is approximately -86dB at 62.5MHz.

Analog input connectors are either SMA or SSMC. If SMA is selected, then only the ADC and DAC connections are available on the module itself. Access to the triggers and clocks is via underside mounted MMCX connectors. A mezzanine board is available that converts from MMCX to SMA (as shown below):



5.1.1 Analog Signal Integrity

The analog signals are embedded in the PCB between ground layers (or top/bottom ground copper areas). This will help prevent cross talk and other noise pickup.

5.1.2 Data Valid

The output of the PLL (used for clocking the ADC) has its frequency measured by the FPGA (with reference to its local clock) and bounds checked to determine whether the clock input to the PLL is within tolerance.

The boundaries are programmable using the I^2C interface.

If the measured frequency is outside of the programmed bounds, then an interrupt can be generated.

When the data is flagged as not valid, then the FRAME signal for the FMC ADC data is set low.

This scheme will detect most circumstances where the clock input could be inadvertently changed or even removed.

5.2 DAC

The module includes a single Analog Devices AD9747 [5] device.

This is a dual 16-bit DAC able to operate from 0 up to 250MSPS. Power dissipation is 355mW maximum (typically 310mW). SFDR is around 82dBc.

The data interface to the FPGA is by means of two 16-bit LVCMOS parallel buses (one per channel). This data is clocked into the FPGA by the DAC signal DCO (Data Clock Output), which is derived from the synthesiser clock to the DAC.

The DAC's internal registers are configured over a 4-wire serial interface from the FPGA.

The analog outputs are DC coupled and provide a 2.2Vpp drive (full scale) into a 50Ω load. Bandwidth is 50MHz (1dB).

Together with additional reset and control pins, a total of 38 FPGA I/O pins are required with a bank voltage of 3.3V.

Output reconstruction filter options are similar to the ADC anti-alias options.

5.3 Clock

Two clock inputs are available for the ADC and DAC clock synthesizers. Either can be chosen via a clock multiplexer. The input amplitude is between -7 and +13dBm with a frequency range of between 8kHz to 200MHz. The clocks inputs have 50 Ohm termination and are AC coupled to a comparator with a hysteresis of +/-100mV.

A fixed crystal can be used in place of the external clock for a specific frequency.

The clocks are input to a PLL based clock generator (e.g. CDCM6208V1) via comparators with hysteresis to provide some tolerance to embedded signal noise. The output frequency range is up to 250MHz. The clocks are also fed directly to the FPGA for error checking and frequency measurement.

RMS Phase jitter is better than 20ps (typically about 1ps).

External clock input amplitude should not exceed 20dBm.

The clock generator outputs are used to drive the ADC/DAC and also the FPGA.

Configuration of the clock generator is performed via I²C interfaces, and as the I²C bus lines are also present on the FMC connector, this configuration can originate from the on-board FPGA OR the DSP board to which the module is attached.

5.4 Triggers

Two external triggers (ESD and over-voltage protected) are provided via comparators (with hysteresis) to LVTTL FPGA inputs. The trigger inputs are DC coupled to a comparator with a hysteresis of +/-100mV centred on 1.4V, so thresholds are 1.3V falling and 1.5V rising.

The triggers' function is defined in the FPGA firmware. Typically this could be used to initiate a data capture, or an interrupt to the FMC carrier.

A maximum repetition rate of 1MHz is supported.

5.5 Connectors

The ADC and DAC inputs and outputs are via SMA connectors on the FMC module. Additional SMA connectors are provided for the clocks and triggers via a small mezzanine card that attaches to the main FMC module via MMCX co-ax connectors.

All of the SMA connectors have a sufficiently long threaded section to allow them to be secured to a front panel using a nut and shake-proof washer.

A build option allows for eight SSMC connectors to replace all of the SMA ones (both on the main FMC and mezzanine boards).

In both the SMA and SSMC cases, a standard FMC front panel can be fitted (not part of the GSI specification as the front panel is part of the custom 19" enclosure).

5.6 FPGA

The SMT-FMC311 is populated with a Xilinx Artix-7 FPGA (XC7A100T-2CSG324I [6], [7]). This device controls major functions on the module, such as FMC communications, data flows to and from the converters, memory and clock management.

The Artix-7 series of FPGAs are designed for low-power applications. This particular device contains 15850 7th generation Xilinx logic slices (63400 2nd generation) 240 DSP slices, and 4860Kb of block RAM. The comparative figure from current ADC/DAC Module and 2nd Generation Xilinx Virtex-2 XC1000 FPGA is 5100.

5.6.1 Configuration

The FPGA needs to be configured after power-up and after a module reset. The FPGA is programmed via the FMC interface and has no local boot PROM.

An I²C I/O expander (e.g. PCA9546) provides the control and status signals to the FPGA. These include PROGRAM_B, DONE and INIT_B. This enables the host FMC carrier to configure the FMC's FPGA at any time.

After the PROGRAM pin has been toggled, the configuration bitstream is sent to the FPGA via the clock and data pins of the SPI bus. The FPGA is then configured using its "Slave Serial Mode" using pins CCLK and DIN.

The following table details the pins used for "Slave Serial Mode" configuration:

PIN Name	Bank	In/Out	Description
M[2:0]	0	In	Set all 3 to VCCO_0 for slave serial mode
DIN	14	In	SPI Serial data in
INIT_B	0	I/O	Input: Pause configuration Output: Signal CRC error
PUDC_B	14	In	Pull up I/Os during configuration when low
PROGRAM_B	0	In	Reset configuration logic when low
CCLK	0	In	Clock serial data
DOUT	14	Out	SPI Serial data out
DONE	0	Out	Configuration complete when high

When using the DIN pin on bank 14, a Xilinx constraint requires that the operating voltage of both bank 14 and bank 15 must match that of bank 0, the dedicated configuration bank. This effectively means that banks 14 and 15 have to have the same supply voltage. Since 2 banks are required to operate at 1.8V, these banks have to be 14 and 15, and all 3 banks (14, 15, 0) have to be supplied with 1.8V.

So that the LVDS SPI data and clock signals can drive the LVCMOS18 FPGA configuration pins DIN and CCLK, a discrete pair of LVDS to LVCMOS18 translators are used, e.g. SN65LVDS4. The outputs of these translators always drive these pins, since CCLK is not used after configuration, and DIN can receive the serial SPI data during normal operation. The DIN pin always receives SPI data. The LVDS SPI clock also drives a standard I/O clock input pair, so the FPGA can clock SPI data in and out.

So that the LVCMOS18 FPGA configuration pin DOUT can drive the LVDS SPI data pair, a discrete LVCMOS18 to LVDS translator is used. The DOUT pin always transmits SPI data. The data from DOUT is not required for configuration, but it does allow loop back confidence testing.

For the pin PUDC_B to be available for general I/O after configuration, it is assigned to an I/O output which drives peripheral inputs that are "do not care" during configuration e.g. an ADC serial interface input. The state of PUDC_B during configuration is determined by a pull up or down resistor.

5.7 SPI

A 4-wire SPI interface is directly coupled to the carrier's FPGA. The SPI chip select provides SPI data framing.

The SPI clock (SCLK) connects to the dedicated FPGA configuration pin CCLK in bank 0 through a discrete LVDS to LVCMOS18 translator, and to a standard LVDS I/O pin pair.

The SPI data (SDO) connects to the dedicated FPGA configuration pin DIN in bank 14 through a discrete LVDS to LVCMOS18 translator. The DIN pin is permanently connected to this translator and always receives SPI data.

5.8 Temperature Sensor

An I^2C temperature sensor with discrete over temperature alarm is fitted, e.g. LM73.

The I^2C bus is routed to the FMC connector, so the carrier the DSP system can read the temperature of the module and send it to a higher-level management system, and set the over temperature alarm level.

The over-temperature condition is signalled via an alarm line which turns off the power supplies to the ADC, DAC, SYNTHESISERS and FPGA core. This over temperature condition does not disable I2C access to the temperature sensor or EEPROM.

5.9 FMC

The FMC connector is the LPC variant (low pin count) which has 34 differential IO pairs, a high-speed gigabit interface, I^2C, JTAG and clocks. Power is provided at 3.3V and 12V and a variable supply VADJ, which is set by the carrier after reading the required voltage from the EEPROM.

The 34 data pairs are split into two data busses of 16 and 8 bits, a 4-wire SPI interface, ADC and DAC frame signals, and an interrupt line. Three pairs are reserved for future expansion and are fully connected. Two differential clocks are also present on the FMC and are routed to the FPGA. The signalling standard is LVDS for all pairs. See the FPGA pin allocation below for more details.

The ADC data is transmitted together with a FRAME signal indicating which of the two ADC channels' data is currently being transmitted.

A similar FRAME signal exists for the DAC interface which is transmitted from the carrier's FPGA.

The FPGA interface pins connected to the FMC LPC use the FMC's variable voltage power pins for I/O bank drive.

The FMC JTAG interface connects directly to the FPGA, so the carrier board can include the FPGA in its JTAG chain.

5.10 LEDs

Four general purpose green LEDs are driven directly from the FPGA. These are visible on the FMC module only and are not presented off-board.

They can be driven in an open-collector type configuration and can thus be placed in any FPGA I/O bank.

5.11 DDR Memory

A single 8Gbit (512M x 16) DDR3 memory is directly connected to the FPGA. This provides a total storage of 1GByte.

This amount of memory is sufficient to store 6s of ADC data (both channels) at a sample rate of 28MSPS.

The DDR3 interface requires 50 I/O pins on the FPGA with a bank voltage of 1.5V.

5.12 Power Supplies

Power is provided at 3.3V and 12V and a variable supply VADJ, directly from the FMC connector. Local voltage rails for the analog components are generated using linear regulators only.

The 12V supply is used to power the analog input and output circuits.

The adjustable FMC supply VADJ is set by the carrier after reading the required voltage from the EEPROM. By selecting a low supply voltage, the FMC board can use only linear regulators, and not require any switching regulators, thus reducing noise sources, while keeping power dissipation low. A typical setting for VADJ is 2.0V, with low dropout linear regulators using it to provide the 1.8V (ADC & FMC) and 1.5V (DDR3) and 1.0V (FPGA core) local low noise supplies.

The FMC power good signal PG_C2M is fed to the FPGA and used as a global reset.

The over-temperature condition signalled via an alarm line from the temperature sensor, turns off the power supplies to the ADC, DAC, SYNTHESISERS and FPGA core. This over temperature condition does not disable I2C access to the temperature sensor or EEPROM.

5.13 JTAG

JTAG signals to the FPGA are routed from the FMC connector. This adds the FMC FPGA into the JTAG chain of the FMC carrier.

When the FMC module is not present, the carrier is responsible for bypassing and keeping the chain intact.

5.14 I²C EEPROM

This is a 2M bit or 256K byte serial EEPROM, and is intended to provide storage for board identification and serialisation, usage data, and other parameters.

Either of the following parts may be used:

Manufacturer	Part number	Data retention years	Write cycle endurance
STM	M24M02	200	4M
ATMEL	AT24CM02	100	1M

As required by the FMC standard, it is powered directly from the supply 3P3VAUX.

It provides data storage to meet the FMC standard, including board information such as manufacturer, part number, serial number, Vadj voltage. A large device is fitted so that if required, analog performance data can be stored, which can potentially be used for digital frequency and phase response correction.

5.15 FPGA Pin-Out by Bank

Inter face	Signal	Standard	FP GA I/O	B14 50x 1V8 24 pairs	B15 50x 1V8 24 pairs	B16 10x 3V3 4 pairs	B34 50x 1V5 24 pairs	B35 50x 3V3 24 pairs	Comment
DDR3	Address: A0-15,BA0-2	SSTL15	O				19		
DDR3	Data: DQ00-15	SSTL15	I/O				16		
DDR3	DQS: LDQS,UDQS	DIFF_SSTL15	O				4		
DDR3	Control: RAS, CAS, WE, CS, ODT, RST, CKE	SSTL15	O				7		
DDR3	Mask: LDM, UDM	SSTL15	O				2		
DDR3	Clock	DIFF_SSTL15	O				2		
LEDs	LED1-4	LVTTL	O					4	
I2C	SCL,SDA	LVTTL	I/O					2	
FMC	ADC_M2C	LVDS	O	16					ADC 8 bit double data rate
FMC	FRAME_M2C	LVDS	O	2					ADC Frame & data valid bit
FMC	DAC_C2M	LVDS	I		32				DAC 16 bit data
FMC	FRAME_C2M	LVDS	I		2				DAC Frame & data valid bit
FMC	SPICLK, SPICS_C2M	LVDS	I	4					
FMC	SPID_C2M	LVCMOS 18	I	1					External discrete LVDS to LVCMOS18
FMC	SPID_M2C	LVCMOS 18	O	1					External discrete LVCMOS18 to LVDS
FMC	Interrupt_M2C	LVDS	O		2				
FMC	(reserved)	LVDS	I/O		6				34 signal pairs on FMC, 3 reserved
FMC	Clock: M2C, C2M	LVDS	O		4				Data clocks
FMC	PG_C2M	LVTTL	I			1			Power good
ADC	Data	LVDS	I	8					2 pairs, 2 channels
ADC	Bit Clock	LVDS	I	2					Bit clock from ADC
ADC	Frame Clock	LVDS	I	2					Frame clock from ADC
ADC	Serial interface: SCLK, SDATA, SEN	LVCMOS 18	O	3					
ADC	Serial	LVCMOS	I	1					

	interface: SDOUT	18							
ADC	Control: RST, PDN	LVCMOS 18	O	2					
DAC	Data: P1D0-15, P2D0-15	LVCMOS 33	O					32	Dual 16 bit data busses
DAC	Clock: DCO	LVCMOS 33	I					1	Data Clock Output from DAC
DAC	Serial interface: SCLK, CSB	LVCMOS 33	O					2	
DAC	Serial interface: SDO, SDIO	LVCMOS 33	I/O					2	
DAC	Reset	LVCMOS 33	O					1	
SYNTH ESISER	Control: REF_SEL0-1, RESET0-1, SYNCN0-1	LVCMOS 18	O	6					
SYNTH ESISER	STATUS0:0-1, 1:0-1	LVCMOS 18	I		4				Includes PLL_UNLOCK
CLOCK	Local 100MHz osc	LVTTL	I			1			
FRONT _PANEL	TRIG1-2	LVTTL	I					2	
FRONT _PANEL	CLOCK1-2	LVTTL	I					2	For error checking only
reserved	reserved	-	-	2		8		2	reserved pins
TOTALS				**50**	**50**	**10**	**50**	**50**	**210**

Notes:

This table is one solution to allocating pins to FPGA banks, and is provided to demonstrate that solutions exist. There are other solutions with equal functionality which may be adopted during detailed design, if required due to other constraints.

This table only shows the allocation of general I/O pins, it does not show any dedicated pins such as the FPGA configuration interface and Bank 0.

Xilinx do not permit allocation of all I/O pins in a bank to differential pairs.

The DDR3 interface is exclusively connected to a single bank powered at 1.5V.

The ADC is powered at 1.8V and has LVDS output levels. This is compatible with any I/O bank when not using internal termination. External termination is used here.

The ADC generates a source synchronous “Bit Clock” which is derived directly from its synthesiser clock, so there is no need to supply the FPGA with the ADC synthesiser clock.

The DAC generates a source synchronous “Data Clock Output” which is derived directly from its synthesiser clock, so there is no need to supply the FPGA with the DAC synthesiser clock.

Signal SPID_C2M is connected to pin DIN in bank 14.

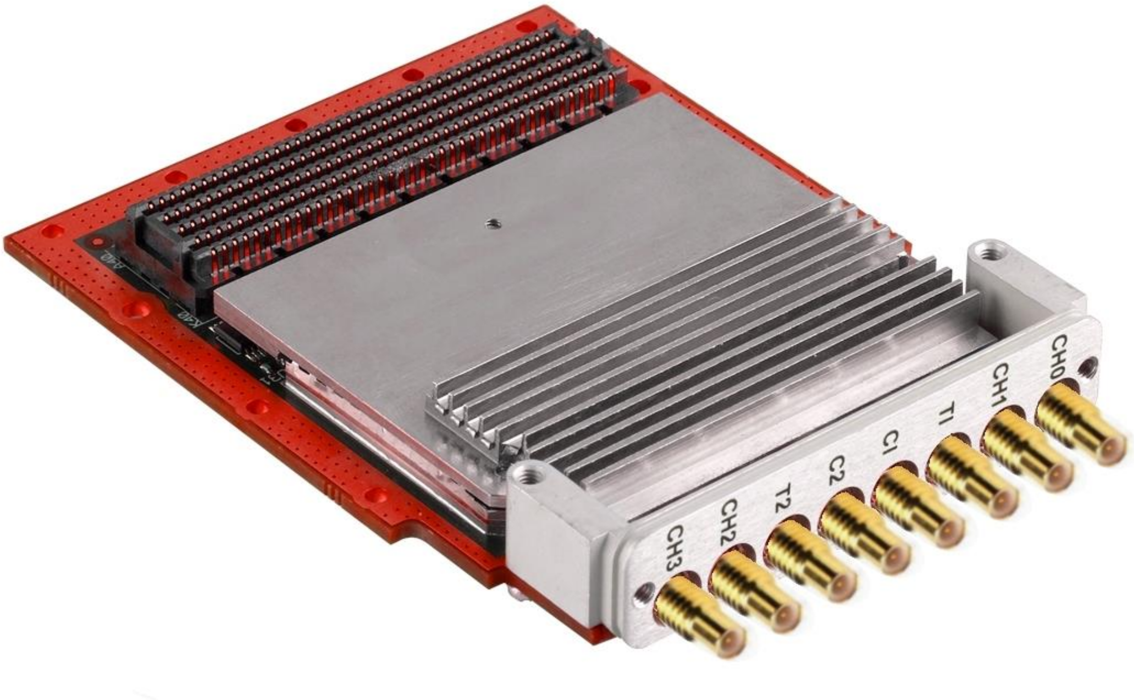
Signal SPID_M2C is connected to pin DOUT in bank 14.

6 Mechanical Design

6.1 Heatsink

Below is a proposed heatsink solution if aircooling is insufficient.

A custom machined heatsink can be mounted directly to the surface of the module's components using thermal compound.



6.2 Conduction Cooled Accessory

In addition to the component mounted heatsink, the FMC module can also be enclosed by thermal rails and a cover to the underside of the module.

The above solution is provided by WaveTherm (www.wavetherm.com).

7 Physical Properties

Dimensions	69mm	88mm

Weight	<400g

Voltage	Power (estimate)
3.3V	1W
12V	250mW
Vadj	1.5W

RH	10-80%
Temperature	0 to +50ºC

MTBF	> 100,000 hours

8 Verification, Review & Validation Procedures

The SMT-FMC311 is a high reliability product, and all design procedures, production and testing maximise product reliability, and are carried out in accordance with the Sundance Quality Procedures (ISO9001).

See: http://www.sundance.com/web/files/static.asp?pagename=quality

9 Safety

This module presents no hazard to the user when in normal use.

10 EMC Statement of Compliance

This module is designed to operate from within an enclosed host system, which is built to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate enclosure.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause a host system to lock up or reboot or result in any permanent damage or other defect.

11 Ordering Information

Order number:

SMT-FMC311-GSI	Comprises of the main FMC board and the SMA mezzanine board. Does not include an FMC panel. Also does not include ADC/DAC filters.
SMT-FMC311-SSMC	FMC main board only fitted with SSMC connectors. Includes an FMC panel and ADC/DAC 4th order filters.