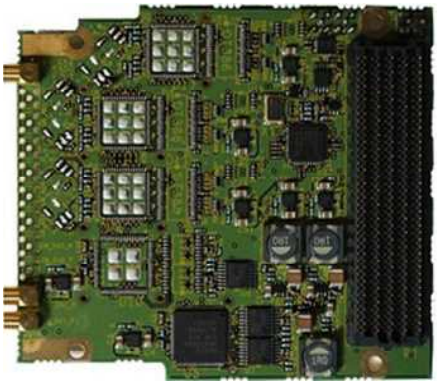
RFM-DACNF01-P500MH
(FMC DA Board)
Hardware Reference Manual
Ver.1.0



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Revision History

Issue	Date	Changes Made
ver1.0	2017/05/23	First Release

Table of Contents

1) Preface

Thank you for choosing **RFM-DACNF01-P500MH** FMC board.
This manual describes the features and specifications of the **RFM-DACNF01-P500MH** FMC board.
Read and understand the contents of this manual before operating this board.

K.K.Rocky reserves the right to revise this document and to make changes without notice.

2) Safety Instructions

Always read the safety instructions carefully.

Cautions

- **If smoke or an abnormal odor is detected from the FMC board, power off and stop using the FMC board.**
  Continuous use of FMC board under these conditions might cause fire or permanent damage to the system. Contact K.K.Rocky to test and repair.

- **Do not attempt to disassemble and modify this board.**
  Disassembly and modification could cause fire or electric shock.
  Please contact K.K.Rocky for any repair and test service.

- **Never allow any liquids to spill on the FMC board, and never expose FMC board to water or moisture**.
  Exposure to liquid or moisture could cause electric shock or fire.

- **Avoid excessive vibration and any impact or shock to the FMC board.**
  Neglect could result in any damage on the board.

- **Avoid handling the FMC board while it is powered. Only handle by the edges to minimize the risk of electrostatic discharge damage.**

- **if the FMC board has been dropped and damaged, stop using the board and contact K.K.Rocky to repair.**

- **Never place the board where it will be exposed to excess heat, such as in direct sunlight, or near heater.**

1. Introduction

The RFM-DACNF01-P500MH is an ANSI/VITA57-1 compliant FPGA Mezzanine Card (FMC) which offers one 16bits DA channel up to 500MSPS.
It works on a High Pin Count (HPC) site of FMC carrier board from K.K.Rocky or third party.

2. Main Components

The main components of the board are listed on Table 2-1.

Table 2-1 Main Components

Item	Description	Remarks
FMC Connector (HPC)	ASP-134488-01 (SAMTEC)	
DA Converter	MAX5888AEGK+D (MAXIM)	
PLL Clock Generator	D9518-3	
EEPROM (I2C)	BR24L01AFV-WE2 (Rohm)	
External Clock Input Connector	MMCX-LR-PC-1 (40) (Hirose)	on Front Panel
External Clock Input Connector	MMCX-R-PC (40) (Hirose)	on Board
(Reference) Mating Cable	RF316-01SP1-03SP1-0500 (SAMTEC)	**This is not shipped with Board**

3. Block Diagram

Figure 3-1 shows the block diagram of the board.

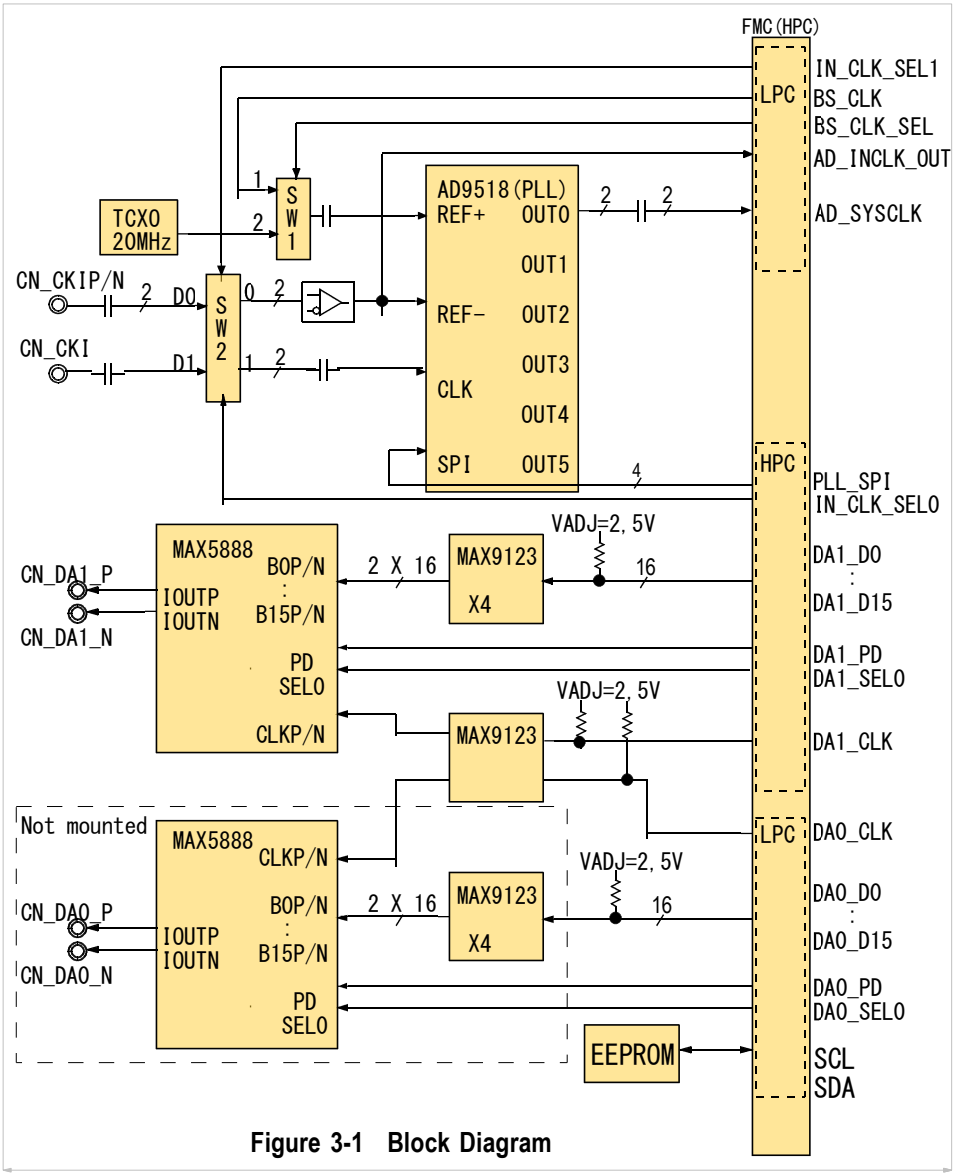

Figure 3-1 Block Diagram

4. Board Layout

Figure 4-1 shows the board layout of RFM-DACNF01-P500MH.

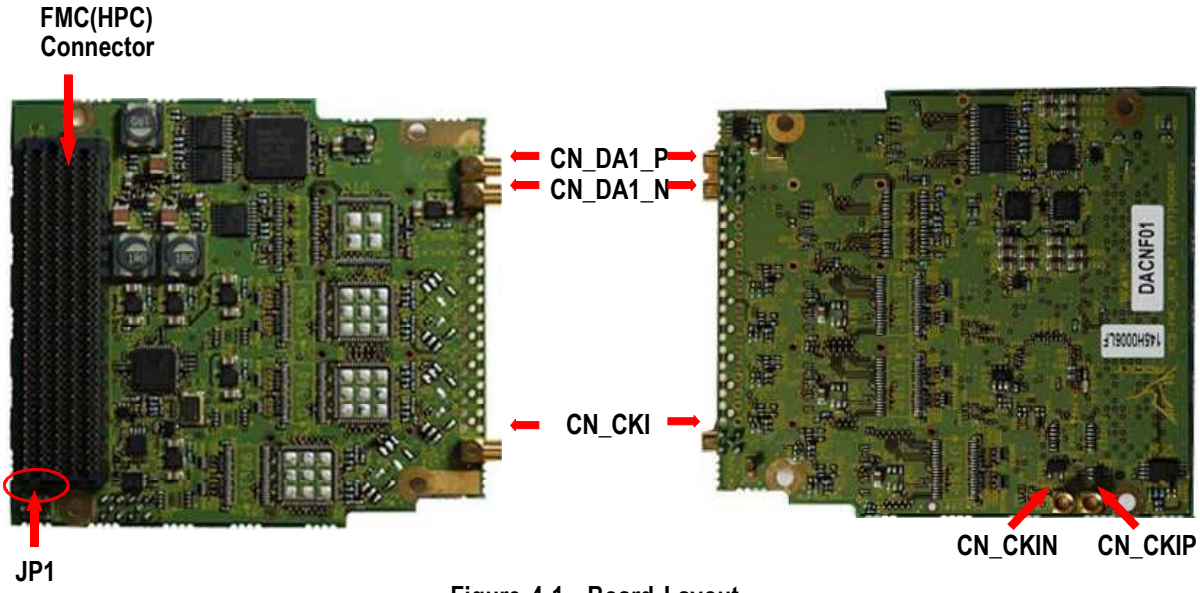

Figure 4-1 Board Layout

Table 4-1 shows the description of connectors.

Table 4-1 Description of connectors

Item	Description	Remarks
FMC Connector	FMC Connector (HPC)	ASP-134488-01 (SAMTEC)
CN_CKI	External Clock Input (Single End)	MMCX-LR-PC-1 (40) (Hirose)
CN_CKIP. CN_CKIN	External Clock Input (Differential)	MMCX-R-PC (40) (Hirose)
CN_DA1_P, CN_DA1_N	Analog output	MMCX-LR-PC-1 (40) (Hirose)

5. Board Specifications

5.1 Output Signals

Table 5-1 shows the specifications of analog output.

Table 5-1 Specifications of Analog output

Item	Description
Number of Output	1 ch
Resolution	16 bit
DA Update Rate (Max)	500Msps
Output Coupling	DC Coupling
Output Impedance	50Ω (Differential)
Output Voltage (Vp-p)	1V (max)

5.2 Power

Table 5-2 shows the required power of the board. All Powers are supplied from FMC carrier board through FMC connector.

Table 5-2 Power

Item	Voltage	Current	Remarks
12P0V	+12V	300mA (Max)	
3P3V	+3.3V	125mA (Max)	
VADJ	+2.5V	85mA (Max)	not include current to VIO_M2C
3P3VAUX	+3.3V	3mA (Max)	

Figure 5-1 shows the block diagram of power distribution.

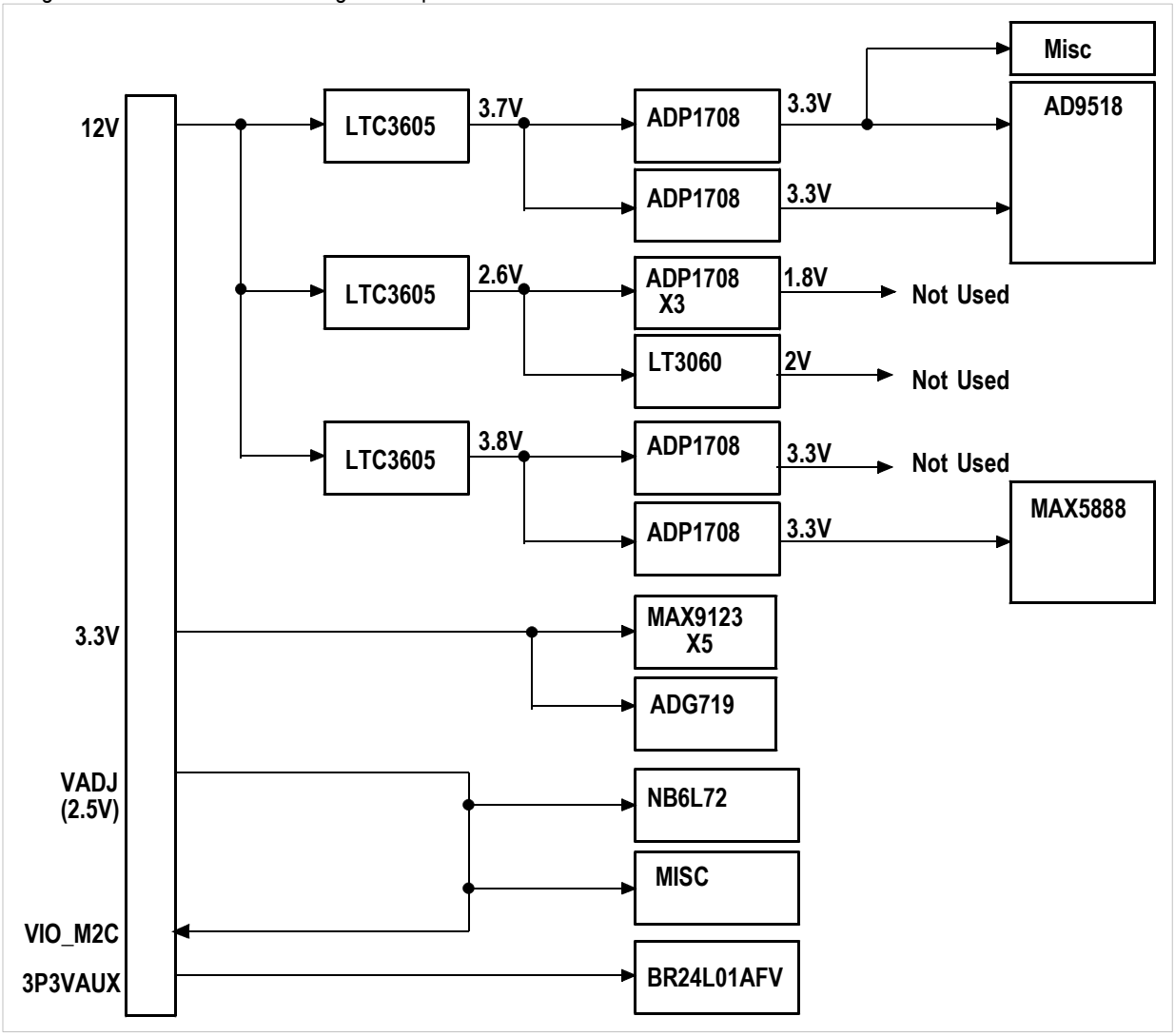

Figure 5-1 Power distribution

5.3 Jumper

Table 5-3 shows the function of JP1.

Table 5-3 JP1 Function

JP1 Setting	Description
Off	Normal Operation (Disable to write EEPROM)
On	Set jumper to enable writing EEPROM

5.4 Signal Flow

Figure 5-2 shows the block diagram of signal flow.

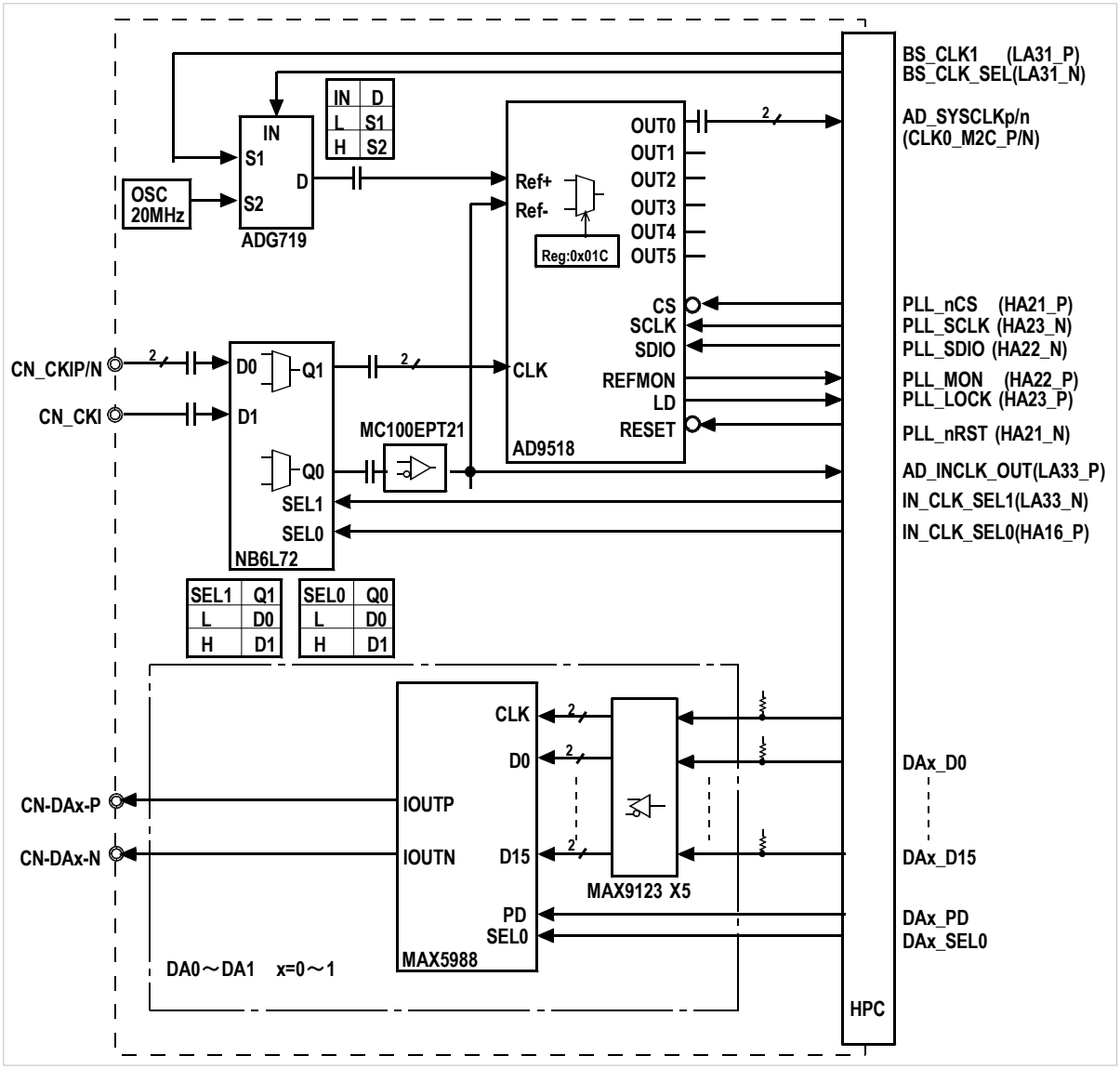

Figure 5-2 Signal Flow Block diagram

DA1 portion is mounted as default for RFM-DACNF01-P500MH.
However DA0 can be mounted as factory option instead of DA1.

5.5 PLL Clock Distribution

Figure 5-3 shows the block diagram of PLL clock distribution.
AD9518-3 clock distribution is described on Table 5-4 and Table 5-5.
Refer to AD9518-3 data sheet for further details of device operation.

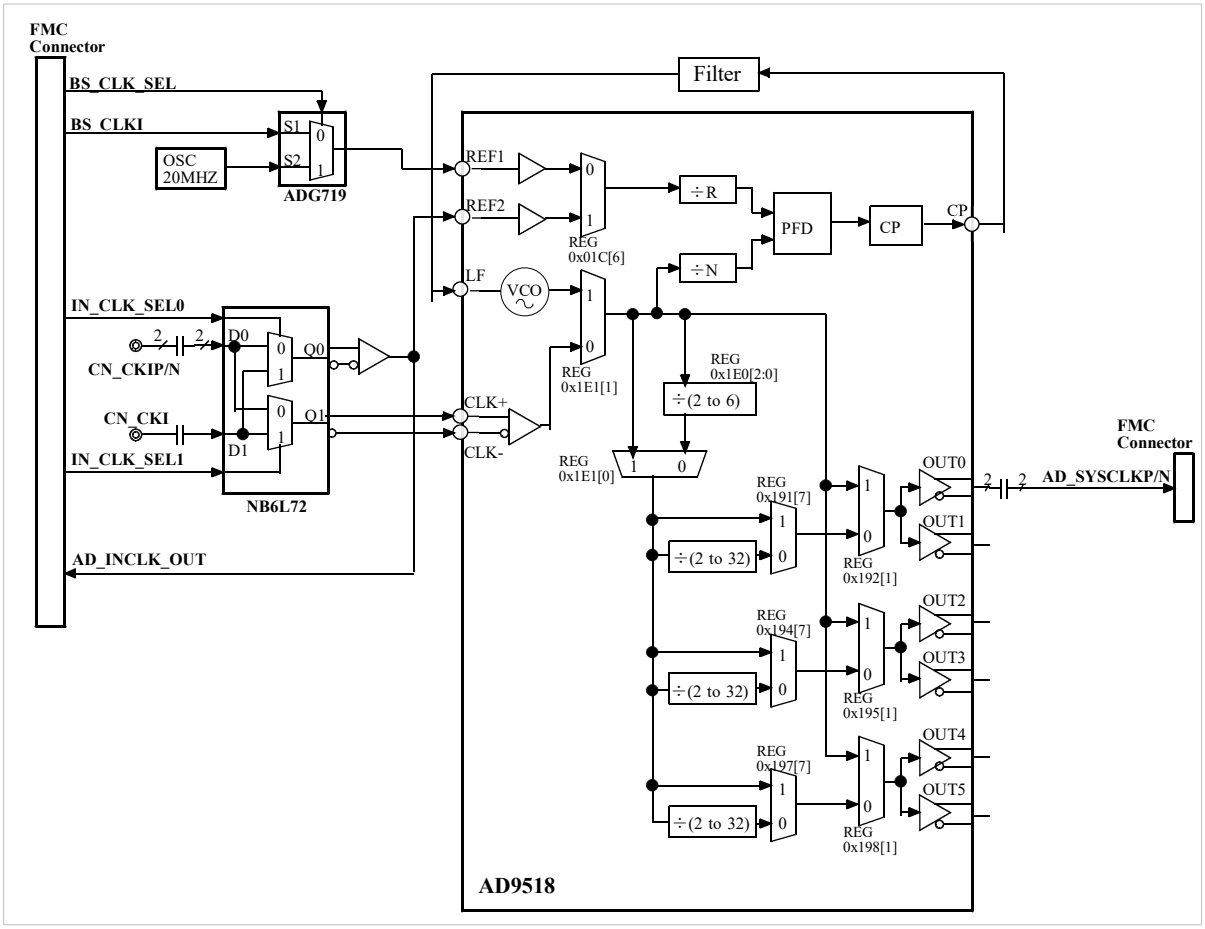

Figure 5-3 The Block Diagram of Clock Distribution

Table 5-4 AD9518-3 PLL Reference source selection (PLL is enabled)

Setting			Remarks	
BS_CLK_SEL	IN_CLK_SEL0	AD9518-3 Register 0x01C[6,2,1]	PLL REF source	Input
H	x	[0,0,1]	TCXO (20MHz)	REF1
L	x	[0,0,1]	BS CLKI (from FMC Carrier)	REF1
x	H	[1,1,0]	CN_CKI (Single ended) on Front Panel	REF2
x	L	[1,1,0]	CN_CKIP/N (Differential) on FMC	REF2

Table 5-5 Sampling Clock Distribution

Clock Source		AD9518-3 Register Setting				AD Clock
		0x1E1[1:0]	VCO Divider	CH Divider	Direct Out	
Internal VCO (fVCO)		[1,0]	2 to 6	1	1	fVCO ÷ (2 to 6)
				2 to 32	0	fVCO ÷{ (2 to 6)×(2 to 32) }
CLK input (fCLK)		[0,0]	2 to 6	1	1	fCLK ÷ (2 to 6)
IN_CLK_SEL1			(f > 1600MHz)	2 to 32	0	fCLK ÷{ (2 to 6)×(2 to 32) }
0	CN_CKIP/N	[0,1]	Bypass	1	0	fCLK ÷ 1
1	CN_CKI		(f < 1600MHz)	2 to 32	0	fCLK ÷ (2 to 32)

5.6 FMC Connector Pin Assignment

Figure 5-4 shows pin assignment of FMC connector.

	K	J	H	G	F	E	D	C	B	A
1	N.C.	GND	N.C.	GND	PG_M2C	GND	N.C.	GND	CLK_DIR	GND
2	GND	N.C.	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	N.C.	GND	N.C.
3	GND	N.C.	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	N.C.	GND	N.C.
4	N.C.	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	N.C.	GND	N.C.	GND
5	N.C.	GND	CLK0_M2C_N	GND	N.C.	GND	N.C.	GND	N.C.	GND
6	GND	HA03_P	GND	N.C.	GND	HA05_P	GND	N.C.	GND	N.C.
7	HA02_P	HA03_N	LA02_P	N.C.	HA04_P	HA05_N	GND	N.C.	GND	N.C.
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	N.C.	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	N.C.	GND	N.C.	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	N.C.
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	N.C.
12	GND	N.C.	GND	LA08_P	GND	N.C.	LA05_N	GND	N.C.	GND
13	HA10_P	N.C.	LA07_P	LA08_N	N.C.	N.C.	GND	GND	N.C.	GND
14	HA10_N.	GND	LA07_N	GND	N.C.	GND	LA09_P	LA10_P	GND	N.C.
15	GND	N.C.	GND	N.C.	GND	HA16_P	LA09_N	LA10_N	GND	N.C.
16	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	GND	GND	N.C.	GND
17	N.C.	GND	N.C.	GND	N.C.	GND	N.C.	GND	N.C.	GND
18	GND	N.C.	GND	N.C.	GND	N.C.	N.C.	N.C.	GND	N.C.
19	HA21_P	N.C.	N.C.	N.C.	N.C.	N.C.	GND	N.C.	GND	N.C.
20	HA21_N	GND	N.C.	GND	N.C.	GND	N.C.	GND	N.C.	GND
21	GND	HA22_P	GND	N.C.	GND	N.C.	N.C.	GND	N.C.	GND
22	HA23_P	HA22_N	N.C.	N.C.	N.C.	N.C.	GND	N.C.	GND	N.C.
23	HA23_N	GND	N.C.	GND	N.C.	GND	N.C.	N.C.	GND	N.C.
24	GND	N.C.	GND	N.C.	GND	N.C.	N.C.	GND	N.C.	GND
25	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	GND	GND	N.C.	GND
26	N.C.	GND	N.C.	GND	N.C.	GND	N.C.	N.C.	GND	N.C.
27	GND	N.C.	GND	N.C.	GND	N.C.	N.C.	N.C.	GND	N.C.
28	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	GND	GND	N.C.	GND
29	N.C.	GND	N.C.	GND	N.C.	GND	N.C.	GND	N.C.	GND
30	GND	N.C.	GND	N.C.	GND	N.C.	TDI	SCL	GND	N.C.
31	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	TDO	SDA	GND	N.C.
32	N.C.	GND	N.C.	GND	N.C.	GND	3P3VAUX	GND	N.C.	GND
33	GND	N.C.	GND	LA31_P	GND	N.C.	N.C.	GND	N.C.	GND
34	N.C.	N.C.	N.C.	LA31_N	N.C.	N.C.	N.C.	GA0	GND	N.C.
35	N.C.	GND	N.C.	GND	N.C.	GND	GA1	12P0V	GND	N.C.
36	GND	N.C.	GND	LA33_P	GND	N.C.	3P3V	GND	N.C.	GND
37	N.C.	N.C.	N.C.	LA33_N	N.C.	N.C.	GND	12P0V	N.C.	GND
38	N.C.	GND	N.C.	GND	N.C.	GND	3P3V	GND	GND	N.C.
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	N.C.
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	N.C.	GND
			LPC Connector				LPC Connector			

Note : N.C. means "No Connection"

Figure 5-4 Connector Pin Assignment

(1) Supply +2.5V to VADJ.
(2) FMC loops back VADJ to VIO_B_M2C.
(3) VREF_A_M2C and VREF_B_M2C are not used (N.C.)
(4) When DA0 is mounted When DA1 is mounted,
When they are not mounted, these pins are N.C.

Table 5-6 shows the signal assignment to FMC connector.

Table 5-6 The Signal Assignment to FMC Connector

Pin#		Signal	FMC_LOC	I/O	Function	Remarks
C	30	SCL	SCL	I	I2C Clock	
C	31	SDA	SDA	I/O	I2C Data	
C	34	GA0	GA0	I	I2C Address 0	
D	35	GA1	GA1	I	I2C Address 1	
When DA1 is mounted (otherwise N.C.)						
K	14	DA1_SEL0	HA10_N	I	DA1 segment shuffling Mode Select	Set High to Activate
K	13	DA1_PD	HA10_P	I	DA1 Power Down	Set Low for normal operation
F	4	DA1_CLK	HA00_P_CC	I	DA1 Clock Input	
K	7	DA1_B0	HA02_P	I	DA1 Data 0 (LSB)	
K	8	DA1_B1	HA02_N	I	DA1 Data 1	
J	6	DA1_B2	HA03_P	I	DA1 Data 2	
J	7	DA1_B3	HA03_N	I	DA1 Data 3	
F	7	DA1_B4	HA04_P	I	DA1 Data 4	
F	8	DA1_B5	HA04_N	I	DA1 Data 5	
E	6	DA1_B6	HA05_P	I	DA1 Data 6	
E	7	DA1_B7	HA05_N	I	DA1 Data 7	
K	10	DA1_B8	HA06_P	I	DA1 Data 8	
K	11	DA1_B9	HA06_N	I	DA1 Data 9	
J	9	DA1_B10	HA07_P	I	DA1 Data 10	
J	10	DA1_B11	HA07_N	I	DA1 Data 11	
F	10	DA1_B12	HA08_P	I	DA1 Data 12	
F	11	DA1_B13	HA08_N	I	DA1 Data 13	
E	9	DA1_B14	HA09_P	I	DA1 Data 14	
E	10	DA1_B15	HA09_N	I	DA1 Data 15 (MSB)	
When DA0 is mounted (otherwise N.C.)						
C	15	DA0_SEL0	LA10_N	I	DA0 segment shuffling Mode Select	Set High to Activate
C	14	DA0_PD	LA10_P	I	DA0 Power Down	Set Low for normal operation
D	8	DA0_CLK	LA01_P_CC	I	DA0 Clock Input	
H	7	DA0_B0	LA02_P	I	DA0 Data 0 (LSB)	
H	8	DA0_B1	LA02_N	I	DA0 Data 1	
G	9	DA0_B2	LA03_P	I	DA0 Data 2	
G	10	DA0_B3	LA03_N	I	DA0 Data 3	
H	10	DA0_B4	LA04_P	I	DA0 Data 4	
H	11	DA0_B5	LA04_N	I	DA0 Data 5	
D	11	DA0_B6	LA05_P	I	DA0 Data 6	
D	12	DA0_B7	LA05_N	I	DA0 Data 7	
C	10	DA0_B8	LA06_P	I	DA0 Data 8	
C	11	DA0_B9	LA06_N	I	DA0 Data 9	
H	13	DA0_B10	LA07_P	I	DA0 Data 10	
H	14	DA0_B11	LA07_N	I	DA0 Data 11	
G	12	DA0_B12	LA08_P	I	DA0 Data 12	
G	13	DA0_B13	LA08_N	I	DA0 Data 13	
D	14	DA0_B14	LA09_P	I	DA0 Data 14	
D	15	DA0_B15	LA09_N	I	DA0 Data 15 (MSB)	

Table 5-6 The Signal Assignment to FMC Connector (continued)

Pin#		Signal	FMC_LOC	I/O	Function	Remarks
F	1	AD_PGOOD	PG_M2C	O	Power Good	
E	2	BS_CLKp	HA01_P_CC	O	Selected External clock	
E	3	BS_CLKn	HA01_N_CC	O	Selected External clock	
G	18	IN_CLK_SEL0	HA16_P	I	CN_CKIP/ CN_CKIN Select	
K	19	PLL_nCS	HA21_P	I	PLL (AD9518) Chip Select	
K	20	PLL_nRST	HA21_N	I	PLL (AD9518) Reset	
J	21	PLL_MON	HA22_P	O	PLL (AD9518) Reference monitor	
J	22	PLL_SDIO	HA22_N	I/O	PLL (AD9518) Serial Control Port data I/O	
K	22	PLL_LOCK	HA23_P	O	PLL (AD9518) Lock detect	
K	23	PLL_SCLK	HA23_N	I	PLL (AD9518) Serial Control port Clock	
H	4	SYSCLKp	CLK0_M2C_P	O	PLL (AD9518) LVPECL Output	
H	5	SYSCLKn	CLK0_M2C_N	O	PLL (AD9518) LVPECL Output	
G	33	BS_CLK	LA31_P	I	PLL Reference Clock from FMC Carrier	
G	34	BS_CLK_SEL	LA31_N	I	Reference Clock Select	Refer to Table 5-4
G	37	IN_CLK_SEL1	LA33_N	I	Input Clock Select	Refer to Table 5-5
G	36	INCLK_OUT	LA33_P	O	Clock Input Monitor	

6. Reference Documents

(1) FPGA Mezzanine Card (FMC) Standard ANSI/VITA 57.1
(2) MAX5888 Data Sheet (MAXIM)
(3) AD9518-3 Data Sheet (Analog Devices)