FMC TDC

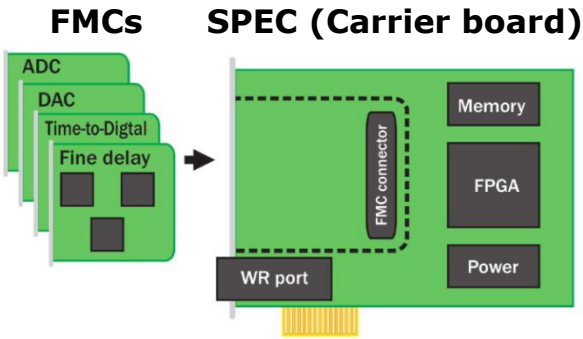
Time to Digital Converter - 1ns 5ch

An FPGA Mezzanine Card (FMC) with a Time to Digital Converter chip to perform one-shot sub-nanosecond time interval measurements

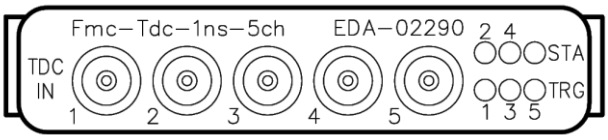
The Time to Digital Converter mezzanine board houses 5 input channels. It can calculate time differences between pulses arriving to the channels with a precision of +-700 ps.

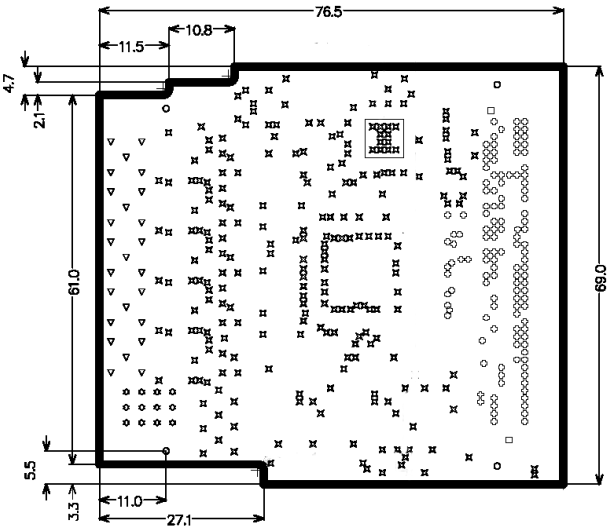
It can be carried by any of the carrier boards: SPEC or SVEC. It is implemented using a dedicated time-to-digital converter IC from the European company ACAM chip in I-mode.

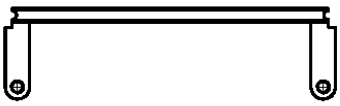
Input	
Channels	5 channels TTL with selectable 50 Ohm termination.
Enabling/Disabling	Software controlled switch
Max. input pulse rate	31.25 MHz from all 5 channels (interrupt notification if rate overpasses this value)
Min input pulse width	100 ns, narrower pulses are ignored on software level by subtracting a falling edge from the previous rising one.
Protection	No protection. Inputs need to be protected against +15V pulses with pulse width > 10us at 50Hz
Timestamps	
Buffer	Circular buffer that keeps the last 128 pulses (256 rising and falling edges); programmable interrupts implemented based on the number of accumulated timestamps or the amount of elapsed time.
Precision	+/- 700 ps deviation
Timebase accuracy	▪ +/- 4 ppm (local TCXO on the FMC board) ▪ Much better when used on a White Rabbit enabled FMC carrier.
ACAM	
Mode	i-mode
Precision	+/- 500ps (6σ)
Resolution	81 ps
Certifications	
Soldering	IPC- 610 Rev E Class 2
Others	ISO-9001, ISO-14001, CE, RoHS
Physical Specification	
Dimension	85,5x69 mm
Weight	

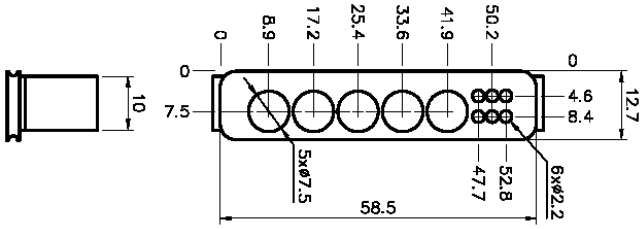


Ilustration of the connection of SPEC with FMCs









info@sevensols.com
(+34) 958 285 024

C/ Baza, parcela 19, nave 3
Polígono Industrial Juncaril,
18210 Peligros (Granada), SPAIN.