FMC DEL 1ns 4cha

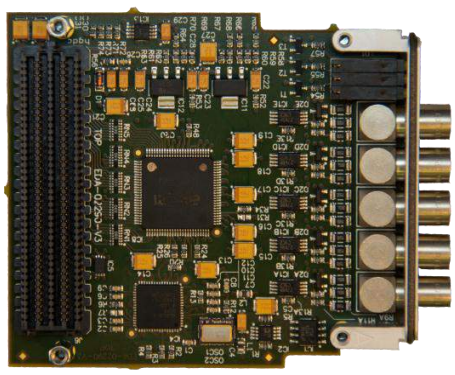
FMC Fine Delay 1ns - 4 ch TTL – 1 ch Trigger

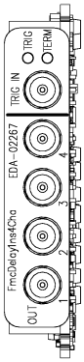
The FMC Delay 1ns-4cha is a 4 output channel FPGA Mezzanine Card (FMC-VITA 57 standard), whose main purpose is to produce pulses delayed by a user-programmed value with respect to the input trigger pulse. Delay can be programmed to any value between 600 ns and 12 seconds with 10 ps resolution. The card can also work as a Time to Digital converter (TDC) or as a programmable pulse generator triggering at a given TAI time. Each single-bit port can be configured individually as input or output. The I/Os that are on LEMO 00 connectors are TTL compatible.

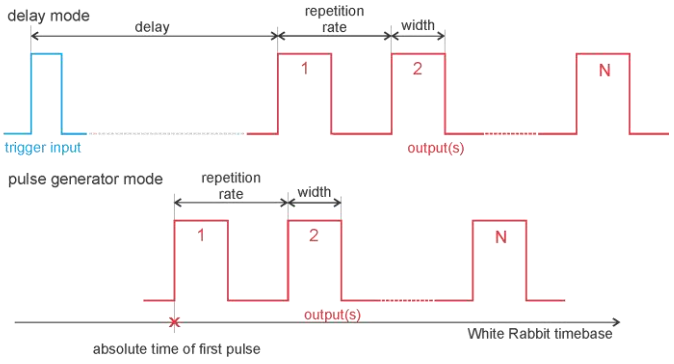
The module can work in one or more of the following modes:

- **Pulse Delay:** produces one or more pulse(s) on selected outputs a given time after an input trigger pulse.
- **Pulse Generator:** produces one or more pulse(s) on selected outputs starting at an absolute time value programmed by the user. In this mode, time base is usually provided by the White Rabbit network.
- **Time to Digital Converter**: tags all trigger pulses and delivers the timestamps to the user's application.

Modes (pulse delay/generator) can be selected independently for each output. The TDC mode can be enabled for the input at any time and does not interfere with the operation of the channels being time tagged.

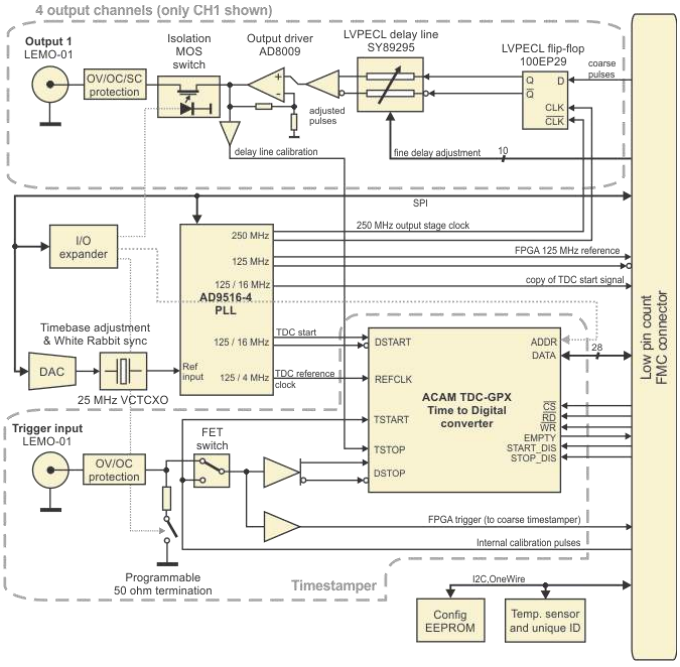


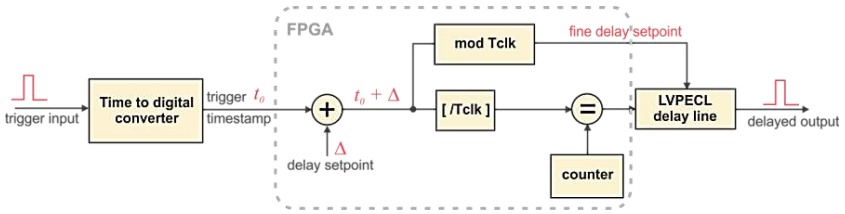




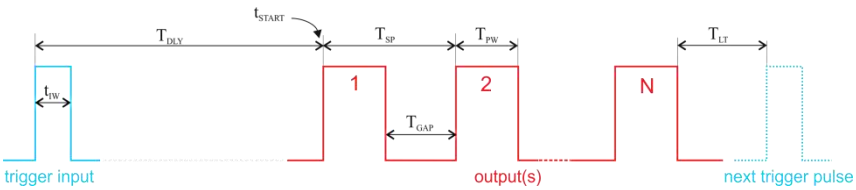
Timing

Time base	▪ +/- 2.5 ppm on-board oscillator accuracy (i.e. max. 2.5 ns error for a delay of 1 ms). ▪ When using White Rabbit as the timing reference depends on the characteristics of the grandmaster clock and the carrier used (on SPEC v4.0 better than 1 ns).
Delay mode specific parameters	▪ < 1 ns Delay accuracy. ▪ 80 ps rms trigger-to-output jitter. ▪ Trigger-to-output delay: $T_{DLY, min}$ = 500 ns, $T_{DLY, max}$ = 120 s. ▪ Maximum trigger pulse rate: T_{DLY} + N (T_{SP} + T_{GAP})+ 100 ns, where N = number of output pulses. ▪ Trigger pulses are ignored until the output with the biggest delay has finished generation of the pulse(s).
Input Timing	▪ 20ns maximum input pulse edge rise time. ▪ Minimum pulse width t_{IW} = 50 ns. Pulses below 24 ns are rejected. ▪ Minimum gap between the last delayed output pulse and subsequent trigger pulse T_{LT} = 50 ns. ▪ Input TDC performance: 400 ps pp accuracy, 27 ps resolution, 70 ps trigger-to-trigger rms jitter (measured at 500 kHz pulse rate).
Output Timing	▪ 10 ps resolution. ▪ Pulse generator mode accuracy 300 ps. ▪ Train generation of 1-65536 pulses or continuous square wave up to 10 MHz. ▪ Output-to-output jitter 10 ps rms (same delay) 30 ps rms (different delays, worst case). ▪ 100 ns - 16 s output pulse spacing (T_{SP} resolution 10 ps steps when T_{PW}, T_{GAP} > 200 ns, otherwise 4 ns). ▪ Output pulse start (t_{START}) resolution: 10 ps for the rising edge of the pulse, 10 ps for subsequent pulses if T_{PW}, T_{GAP} > 200 ns, otherwise 4 ns.



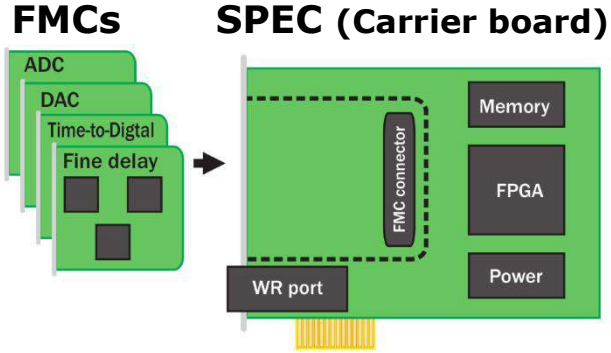


Simplified principle of Fine Delay operation

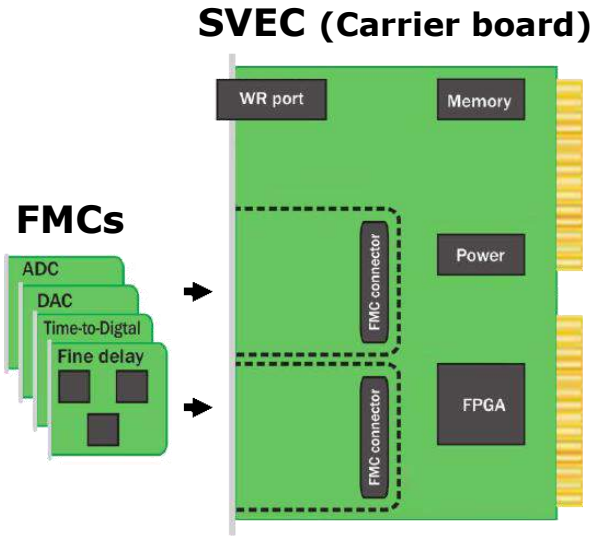


Fine Delay timing parameter definitions

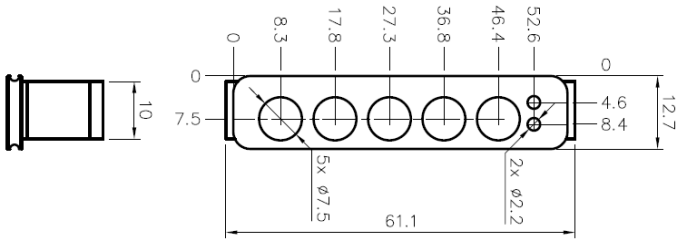
Output	
Connector	4 pulse outputs LEMO 00
Levels	TTL-compatible levels DC-coupled: V_{oh} = 3 V, V_{ol} = 200 mV (50 Ohm load), V_{oh} = 6V, V_{ol} = 400 mV (high impedance).
States	Power-up state: LOW (2 kOhm pulldown), guaranteed glitch-free
Rise/fall	2.5 ns (10% - 90%, 50 Ohm load)
Protection	Protected against continuous short circuit, overcurrent and overvoltage (up to +28 V).
Trigger Input	
Connector	1 trigger input LEMO 00
Levels	TTL/LVTTL levels, DC-coupled.
Thresholds	2 kOhm or 50 Ohm input programmable impedance (indicated by the "TERM" LED)
Bandwidth	1 MHz (minimum pulse spacing: 1 us)
Power-up input impedance	2 kOhm
Protection	Protected against short circuit, overcurrent (> 200 mA) and overvoltage (up to +28 V).
Certifications	
Soldering	IPC- 610 Rev E Class 2
Others	ISO-9001, ISO-14001, CE, RoHS
Environmental Conditions	
Temperature	0ºC ~ +90ºC
Humidity	0% ~ 90% RH

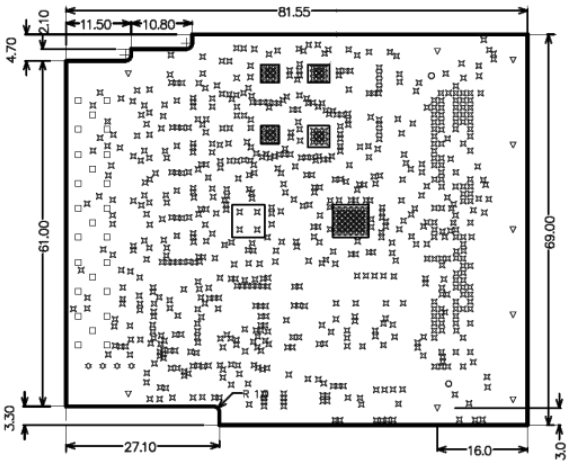


Ilustration of the connection of SPEC with FMCs



Ilustration of the connection of SVEC with FMCs





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