

VF360 User Manual

03010-05093

Rev. 0D



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Revision History

Revision	Date	Changes
0A	December 2014	First Draft release
0B	January 2015	Added FPGA configuration and programming information Added high power requirement Added DSP PCIe mode description, BIOS commands and vf360mon description Added DSP interface diagram and description
0C	February 2015	Added VPX pin connections Cosmetics
0D	December 2015	Added FMC to FPGA information Added FPGA speed grade options and 8-core DSP variant Added DSP Boot options & updated BIOS settings table Updated Power table (Table 2) and VPX P1 User Defined pins (Figure 5)

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About This Manual

This manual consists of information to simplify your installation, configuration and operation of the VF360 board. *About this Manual* describes the contents of each chapter and includes document conventions and technical support information

Chapters Overview

About This Manual - This chapter provides an overview of the chapters, document conventions, and technical support information.

Chapter 1 Introduction - This chapter provides a brief introduction to the VF360 3U FPGA and DSP OpenVPX Processing Module. It also provides a list of reference documents whose information supplements this user manual.

Chapter 2 Product Overview - This chapter provides detailed functional information for the VF360.

Chapter 3 Specifications - This chapter provides the specifications for the functional areas of the VF360.

Chapter 4 Installation and Setup - This chapter includes instructions for unpacking and installing the VF360.

Chapter 5 Operating Guide - This chapter provides information on proper operation of the VF360.

Chapter 6 Monitor, BIOS & GPIOs - This chapter describes the VF360 BIOS settings and the DSP GPIO usage.

Acronym List - This chapter expands abbreviations used in this manual.

Document Conventions

The following icons are used in this manual to emphasize setup or system information:

Icon	Use
	Alerts you to the important details regarding the setup and maintenance of your system.
	Alerts you to potential damage to the board during system setup and installation.

Technical Support

Should you require additional technical information or assistance, contact Parsec (Pty) Ltd:

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1 Introduction

This chapter provides a brief introduction to the VF360 3U FPGA and DSP OpenVPX Processing Module. It also provides a list of reference documents whose information supplements this user manual.

1.1 The VF360 OpenVPX FPGA & DSP Processing Module

The VF360 is a 3U OpenVPX module that leverages on ALTERA Stratix® V FPGA and Texas Instruments KeyStone Multicore DSP technology to provide an ultra-high bandwidth processing platform, ideally suited for computation and bandwidth intensive applications such as Radar, Networking, SIGINT, EW, SDR and Video.

The VF360 uses an ALTERA Stratix® V GX/GS FPGA device to implement a high-speed processing node. The FPGA is available to the user for custom firmware development. Depending on the FPGA resources required, one of ten different FPGAs from the Stratix® V GX and GS families can be mounted on the VF360.

The Stratix® V FPGA has two banks of dedicated DDR3 and QDRII+ memories for algorithms with high bandwidth and/or large memory size requirements. High-speed serial interfaces to the OpenVPX data plane and the FMC site creates abundant FPGA IO throughput.

The on-board KeyStone Multicore C667X DSP processor from Texas Instruments provides the flexibility to perform complex post processing functions more suitable for the processor domain. High bandwidth communication between the DSP and FPGA is provided through both PCIe and Serial Rapid IO (SRIO) interfaces.

The VF360 acts as an FMC carrier to provide a modular solution that accommodates a wide range of I/O requirements.

The VF360 conforms to the OpenVPX standard and operates as a Payload module with System Controller capability. Both air-cooled and conduction cooled versions are available.

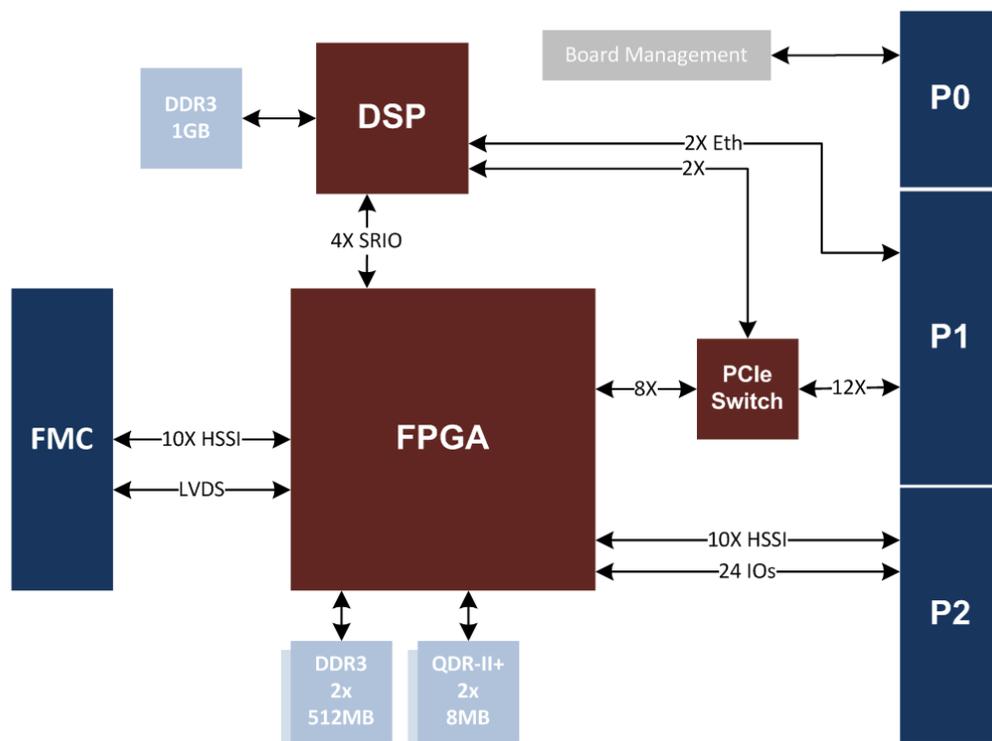


Figure 1: VF360 Block Diagram

1.2 Features

❖ High speed FPGA processing with ALTERA Stratix® V GX/GS FPGA

GX Device variants: 5SGXA3, 5SGXA4, 5SGXA5, 5SGXA7, 5SGXA9 and 5SGXAB

GS Device variants: 5SGSD4, 5SGSD5, 5SGSD6 and 5SGSD8

Embedded device memory: 19-52 MBits

Embedded device multipliers (18x18) : 512 – 3,926

❖ FPGA external DDR and QDR memory

Up to 2GB DDR3 @ 667MHz (arranged as two 256M x 32-bit banks), default 1GB

Up to 32MB QDRII+ SRAM @ 400MHz (arranged as two 8M x 18-bit banks), default 16MB

❖ High speed DSP processing with Ti KeyStone Multicore C667X DSP processor

DSP variants: One, two, four (standard) or eight cores @ 1GHz

DSP dual-boot option for Linux or 2nd boot OS (e.g. SYS/BIOS or other RTOS)

❖ DSP external DDR memory

Up to 2 GB DDR3 @ 667MHz (matched to FPGA DDR3 size), default 1GB

❖ DSP and FPGA is connected through PCIe (x2) and Serial Rapid IO (SRIO x4) interfaces

❖ VITA 57 FPGA MEZZANINE CARD (FMC) site

10x High-Speed Serial Interface (HSSI) lanes

58x Differential LVDS interfaces on LA and HA

❖ VPX INTERFACE

Comply with OpenVPX MOD3-PAY-3F2U-16.2.12-2 module profile

- PCIe Gen2 Data plane (3x Fat Pipes)
- GigE 1000BASE-BX Control plane (2x Ultra-Thin Pipes)
- Payload module with System Controller capability

Supports FPGA configurable User I/O on P2

- 10x High-Speed Serial Interface lanes
- 24x single-ended 2.5V LVCMOS I/Os

❖ FPGA configuration

Automatic configuration of FPGA after power-up from on-board non-volatile storage

DSP can configure FPGA from an RBF file

❖ SOFTWARE & FIRMWARE SUPPORT

Linux distribution and BSP (Board support package)

- PCIe driver for FPGA with DMA support
- EP (endpoint) 'driver' for DSP in 'slave' (Payload module) mode
- Test application showing FPGA memory access and PCIe DMA

- Software Reference Manual

FPGA Firmware Reference Design

- PCIe interface with Read/Write and DMA
- DDR3 and QDRII+ memories connected to QSYS fabric
- High-Speed Serial Interface (HSSI) block connected to SERDES links
- Quartus Project files
- Firmware Reference Manual

❖ Custom FPGA firmware /application /driver development available upon request

❖ FMC COMPANION MODULES

FM500 Test FMC with USB-Blaster II, XDS100 and mini-SAS interface

FM510 Video IO FMC with HD (3G-SDI) video, SD (Analogue) video, RS422, RS485, CAN, Digital IOs & stereo Audio interfaces

FM550 FMC with Dual mini-SAS interface

VR300 Test RTM with USB-Blaster II, XDS100 and Ethernet (via SFP)

1.3 Product Applications

The VF360 is targeted at applications requiring the following:

- Ultra-high bandwidth ($\geq 10\text{Gbps}$) full-duplex serial I/O requirements
- High bandwidth ($\geq 500\text{MB/s}$) PCIe data throughput
- High concentration DSP processing resources
- High-speed FPGA processing
- Real-time DSP processing

A few typical applications well suited for the VF360 platform are:

- Real-time DSP functions (DDC, FFT, FIR, etc.)
- Video and Image Processing functions (Symbology, DCT, 1D/2D Convolution, etc.)
- Radar Signal Processing (Doppler filter, Pulse compression, CFAR, etc.)
- Spectrum analysis in EW (Signal detection & classification, jammer control)
- Software Defined Radio (SDR)

1.4 Reference Documents

The following sources provide important reference information that may provide useful in achieving optimal operation of the VF360:

- [1] VF360 Software Reference Manual
- [2] VF360 Firmware Reference Manual
- [3] FM500 FMC Product Brief
- [4] VR300 RTM Product Brief
- [5] ALTERA STRATIX® V Device Handbook

2 Product Overview

This chapter provides detailed functional information for the VF360.

2.1 Overview of the VF360

The VF360 is a 3U OpenVPX module that leverages on ALTERA Stratix® V FPGA and Texas Instruments KeyStone Multicore DSP technology to provide an ultra-high bandwidth processing platform, ideally suited for computation and bandwidth intensive applications such as Radar, Networking, SIGINT, EW, SDR and Video.

Figure 2 shows an architecture diagram of the VF360 in its standard configuration.

- ❖ The Board Management function powers up the VF360 and boots the DSP Core0
- ❖ The FPGA boots from on-board non-volatile memory (an EPCQ device)
- ❖ Core0 boots the Linux kernel and performs PCIe enumeration when the VF360 is a System Controller. Cores 1-3 are available to run code in the TI SYS/BIOS environment
- ❖ The FPGA Reference Firmware connects the DDR and QDR memories to the DSP via the PCIe and SRIO interfaces. The PCIe and SRIO share the same FPGA memory map

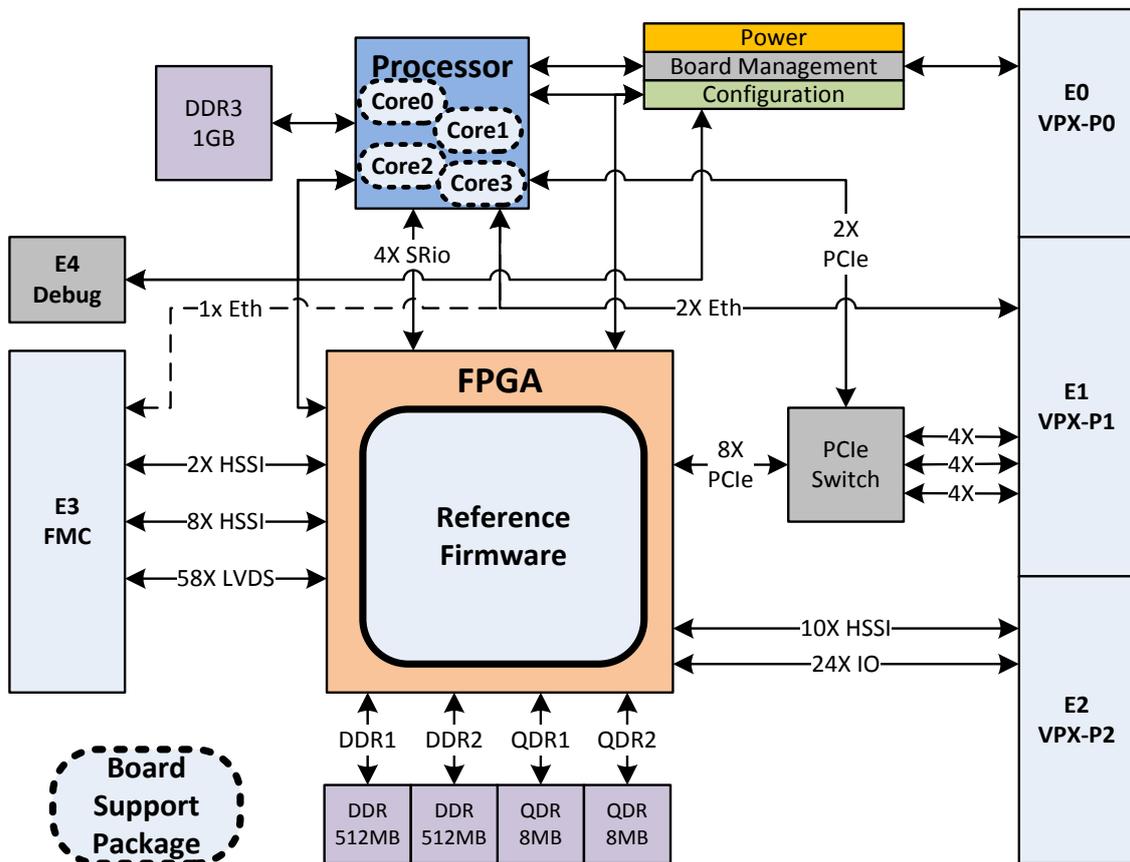


Figure 2: VF360 System architecture diagram

2.2 Board Management

The VF360 Management Controller (MANCON), an Atmel ATXMega device, performs the following functions:

- ❖ Monitors external power supplies (VS1=12V, VS2=3.3V and VS3=5V) for correct levels
- ❖ Enables local power supplies
- ❖ Performs reset actions (nSYSRESET and local resets)
- ❖ Continuously monitors external voltages and local voltages and temperatures
 - Communicates voltages and temperatures and other information to the DSP Linux host
 - Shuts-down VF360 if any power supply or device temperature is out of its operating limits.
 - Logs internal shut-down event in non-volatile memory

The voltages and temperatures communicated to the DSP Linux host running on Core0, are served over Ethernet by the VF360 Monitor application (**vf360mon**) service running on Linux.

Refer to § 6.1 for detail on the **vf360mon** commands.

VF360mon also provides access to the VF360 BIOS options, for more detail refer to § 6.2.

2.3 VPX Interface

The VF360 complies with the 3U OpenVPX slot profile SLT3-PAY-3F2U-14.2.13 as shown in Figure 3.

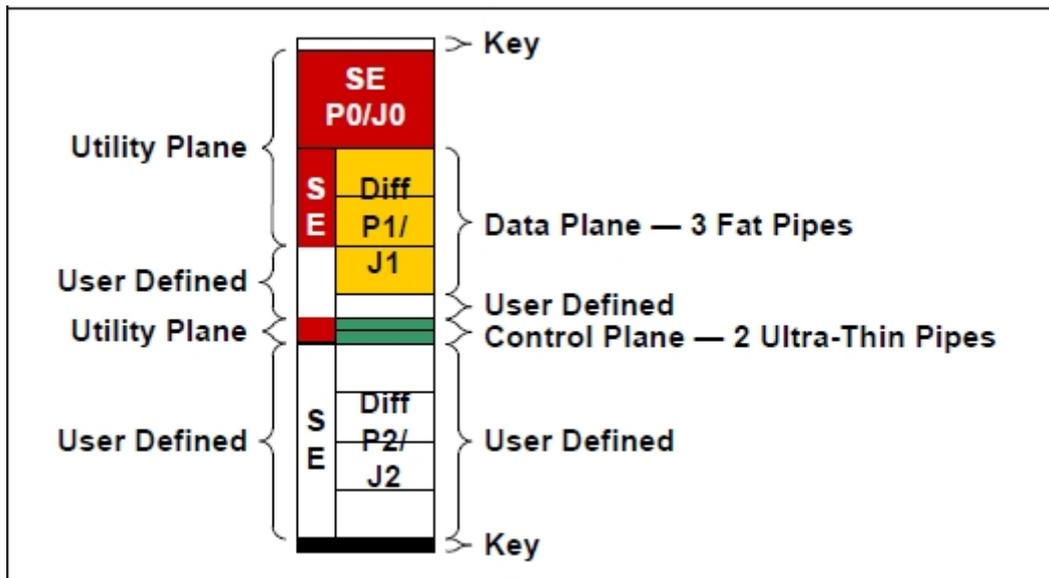


Figure 14.2.13-1 Payload Slot Profile SLT3-PAY-3F2U-14.2.13

Figure 3: VF360 Slot Profile

The VF360 standard module profile (**MOD3-PAY-3F2U-16.2.12-2**) provides the following VPX interfaces:

- ❖ P0 as per ANSI/VITA65 OpenVPX
- ❖ 3x PCIe **Gen2** Data plane Fat Pipes (4X) on DP01 to DP03
MOD3-PAY-3F2U-16.2.12-1 is also supported with PCIe **Gen1** on the Data plane
- ❖ Two GigE 1000BASE-BX Control plane Ultra-Thin Pipes on CPutp01 to CPutp02
- ❖ P2 User Defined connections according to ANSI/VITA46.9 Pin Field **X24s+X8d+X12d**
 - 20 Differential pair IOs
 - 24 Single-ended IOs

As shown in Figure 13, the P2 User Defined signals connect to FPGA transceiver bank R(0-2) and IO bank 4D.

The following three figures show the VF360 connector and Backplane connector pin assignments.

	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1 (12V)	Vs1 (12V)	Vs1 (12V)	No Pad	Vs2 (3.3V)	Vs2 (3.3V)	Vs2 (3.3V)
2	Vs1 (12V)	Vs1 (12V)	Vs1 (12V)	No Pad	Vs2 (3.3V)	Vs2 (3.3V)	Vs2 (3.3V)
3	Vs3 (5V)	Vs3 (5V)	Vs3 (5V)	No Pad	Vs3 (5V)	Vs3 (5V)	Vs3 (5V)
4	SM2	SM3	GND	Reserved (-12V_Aux)	GND	SYSRESET*	NVMRO
5	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1
6	GA3*	GA2*	GND	Reserved (+12V_Aux)	GND	GA1*	GA0*
7	TCK	GND	TDO	TDI	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	AUX_CLK-	AUX_CLK+	GND

Figure 4: VPX P0 Slot Profile assignments

Plug-in module P1		Row G	Row F	Row E		Row D	Row C	Row B		Row A
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1 X8 1x4 / 2x2 / 4x1	GDiscrete1	GND	GND-J1	DP01-TD0-	DP01-TD0+	GND	GND-J1	DP01-RD0-	DP01-RD0+
2		GND	DP01-TD1-	DP01-TD1+	GND-J1	GND	DP01-RD1-	DP01-RD1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-TD2-	DP01-TD2+	GND	GND-J1	DP01-RD2-	DP01-RD2+
4		GND	DP01-TD3-	DP01-TD3+	GND-J1	GND	DP01-RD3-	DP01-RD3+	GND-J1	GND
5	Data Plane Port 2 X8 1x4 / 2x2 / 4x1	SYS_CON*	GND	GND-J1	DP02-TD0-	DP02-TD0+	GND	GND-J1	DP02-RD0-	DP02-RD0+
6		GND	DP02-TD1-	DP02-TD1+	GND-J1	GND	DP02-RD1-	DP02-RD1+	GND-J1	GND
7		Reserved	GND	GND-J1	DP02-TD2-	DP02-TD2+	GND	GND-J1	DP02-RD2-	DP02-RD2+
8		GND	DP02-TD3-	DP02-TD3+	GND-J1	GND	DP02-RD3-	DP02-RD3+	GND-J1	GND
9	Data Plane Port 3 X8 1x4 / 2x2 / 4x1	UDEB-TX	GND	GND-J1	DP03-TD0-	DP03-TD0+	GND	GND-J1	DP03-RD0-	DP03-RD0+
10		GND	DP03-TD1-	DP03-TD1+	GND-J1	GND	DP03-RD1-	DP03-RD1+	GND-J1	GND
11		UDEB-RX	GND	GND-J1	DP03-TD2-	DP03-TD2+	GND	GND-J1	DP03-RD2-	DP03-RD2+
12		GND	DP03-TD3-	DP03-TD3+	GND-J1	GND	DP03-RD3-	DP03-RD3+	GND-J1	GND
13	User Def.	UDSPR-SE	GND	GND-J1	UDMDCLK	UDMDIO	GND	GND-J1	UDUSB-	UDUSB+
14		GND	UDID-CS	UDID-CK	UDID-DO	UDID-DI	GND	GND-J1	GND	GND
15	Control Plane	Maskable Reset*	GND	GND-J1	CPutp02-TD-	CPutp02-TD+	GND	GND-J1	CPutp02-RD-	CPutp02-RD+
16		GND	CPutp01-TD-	CPutp01-TD+	GND-J1	GND	CPutp01-RD-	CPutp01-RD+	GND-J1	GND

Figure 5: VPX P1 & J1 Slot Profile assignments

UDEB-TX/RX is the DSP debug serial port.

UDUSB+/- is the USB interface for the FPGA USB-Blaster II via the VR300 RTM.

UDMDCLK/MDIO connects to the MDIO bus of the DSP

UDID(CK, CS, DI & DO) are 2.5V FPGA IOs that connect to the EEPROM on the VR300 RTM for ID information

UDSPR-SE is a single-ended spare line that connect to a 2.5V FPGA Bank (4D)

Plug-In Module P2	Row G	Row F	Row E		Row D	Row C	Row B		Row A	
			Even	Odd			Even	Odd		
Bplane J2	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a	
1	X24s	UDTCK	GND	GND-J2	X24s23	X24s21	GND	GND-J2	X24s24	X24s22
2		GND	X24s19	X24s17	GND-J2	GND	X24s20	X24s18	GND-J2	GND
3		UDTDO	GND	GND-J2	X24s15	X24s13	GND	GND-J2	X24s16	X24s14
4		GND	X24s11	X24s09	GND-J2	GND	X24s12	X24s10	GND-J2	GND
5		UDTDI	GND	GND-J2	X24s07	X24s05	GND	GND-J2	X24s08	X24s06
6		GND	X24s03	X24s01	GND-J2	GND	X24s04	X24s02	GND-J2	GND
7	X8d	UDTMS	GND	GND-J2	X8d01-TD-	X8d01-TD+	GND	GND-J2	X8d01-RD-	X8d01-RD+
8		GND	X8d02-TD-	X8d02-TD+	GND-J2	GND	X8d02-RD-	X8d02-RD+	GND-J2	GND
9		UDTRST*	GND	GND-J2	X8d03-TD-	X8d03-TD+	GND	GND-J2	X8d03-RD-	X8d03-RD+
10		GND	X8d04-TD-	X8d04-TD+	GND-J2	GND	X8d04-RD-	X8d04-RD+	GND-J2	GND
11	X12d	UDEM0	GND	GND-J2	X12d01-TD-	X12d01-TD+	GND	GND-J2	X12d01-RD-	X12d01-RD+
12		GND	X12d02-TD-	X12d02-TD+	GND-J2	GND	X12d02-RD-	X12d02-RD+	GND-J2	GND
13		UDEM1	GND	GND-J2	X12d03-TD-	X12d03-TD+	GND	GND-J2	X12d03-RD-	X12d03-RD+
14		GND	X12d04-TD-	X12d04-TD+	GND-J2	GND	X12d04-RD-	X12d04-RD+	GND-J2	GND
15		UDJSEL*	GND	GND-J2	X12d05-TD-	X12d05-TD+	GND	GND-J2	X12d05-RD-	X12d05-RD+
16		GND	X12d06-TD-	X12d06-TD+	GND-J2	GND	X12d06-RD-	X12d06-RD+	GND-J2	GND

Figure 6: VPX P2 & J2 Slot Profile assignments

UDTxx and UDEMU[1:0] is the DSP emulator lines on the XDS100

UDJSEL* is an active low select line, indicating that the XDS100 USB cable is plugged into the VR300 RTM.

2.4 DSP interfaces

The DSP interfaces to the FPGA and other related devices are shown in Figure 7.

DSP local resets, NMI, GPIO[13:0], SRIO[3:0], TimI[1:0], TimO[1:0] and SPI interface on CS1 connects to the FPGA. GPIO[0] is used to reset the FPGA.

The FPGA can be configured by the DSP, after initial power-up configuration, through the DSP's SPI interface. For detail refer to 5.3.5.

The PCIe interface connects to the PCIe Switch and the two SGMII interfaces (Ethernet) connect to the VPX Control Plane.

The DSP reset and booting is controlled by MANCON via the Control CPLD.

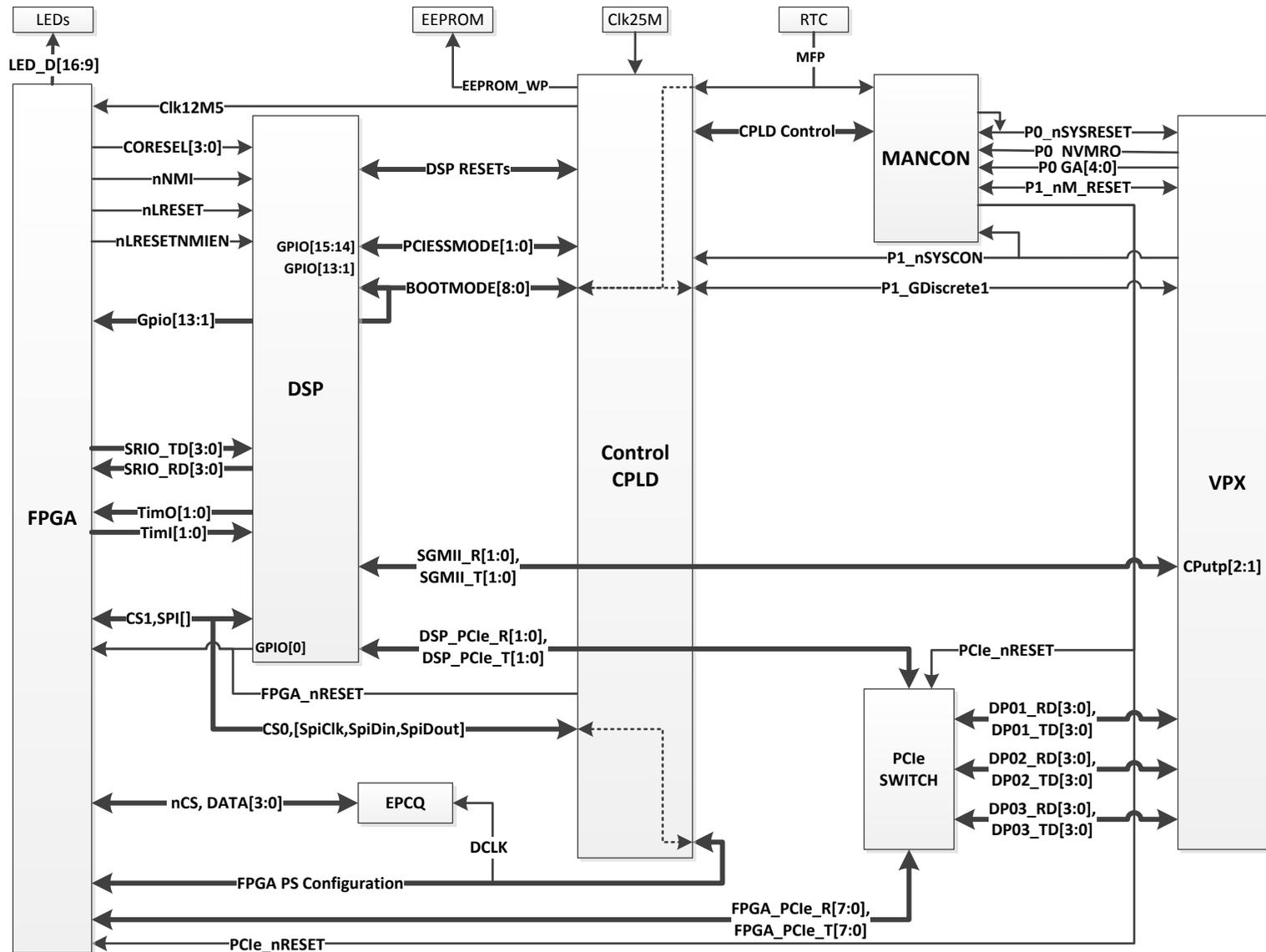


Figure 7: VF360 DSP interfaces

2.5 FPGA Interfaces

The FPGA interfaces are shown in Figure 2 and Figure 7 and are described in more detail in the following sections. For detail on the FPGA interface pin mappings, refer to [2].

2.5.1 DSP Interface

Refer to 2.4.

2.5.2 FMC Interface

The VF360 support the ANSI/VITA 57.1 FPGA Mezzanine Card (FMC) high-pin count (HPC) connector with the following connections to the FPGA, as shown in Figure 8. The FMC_HB[0:21]p,n signals are not provided for.

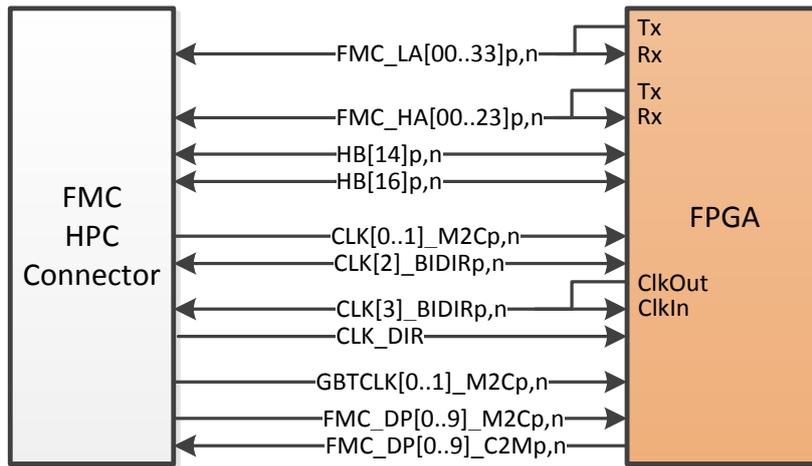


Figure 8: VF360 FMC FPGA signals

⚡ The **maximum input voltage** on FPGA signals from the FMC is **2.5V**. The VF360 **does not support 3.3V** on its FMC interface signals.

Descriptions of the FPGA FMC signals are shown in Table 1.

Table 1: VF360 FPGA FMC signals

Signal	FPGA Pins	I/O Standard	Description
LA[00..33]p LA[00..33]n	2x 68	2.5V or LVDS	Differential pairs or single-ended signals to/from FPGA
HA[00..23]p HA[00..23]n	2x 48	2.5V or LVDS	Differential pairs or single-ended signals to/from FPGA
HB14p, HB14n, HB16p, HB16n	4	2.5V	Single-ended signals to/from FPGA
CLK[0..1]_M2Cp,n	4	LVDS	Two Differential Clocks from FMC to FPGA
CLK[2..3]_BIDIRp,n	4	LVDS	Two Bidirectional differential clocks between FMC and FPGA
CLK_DIR	1	2.5V	Direction signal for CLK[2..3]_BIDIR
GBTCLK[0..1]_M2C	4	CML / LVDS	FPGA Reference clock inputs for FMC transceiver signals DP[0..9]
DP[0..9]_M2C	20	CML	10x HSSI transceiver inputs on FPGA
DP[0..9]_C2M	20	CML	10x HSSI transceiver outputs on FPGA

For detail on specific clock connections between the FMC and FPGA, refer to Figure 13. For detail on the HSSI connections between the FMC and FPGA, refer to Figure 11.

Note that the FMC_LA[] and FMC_HA[] signals connect to LVDS transmitter (Tx) and LVDS receiver (Rx) pins on the FPGA, since the FPGA LVDS pins are uni-directional.

2.5.3 DDR memories

The VF360 FPGA is connected to 1GByte of DDR3 memory, arranged as two banks of 128M x 32-bit memory running at 400MHz (standard build). The two DDR banks are completely independent with separate clock, control address and data lines as is shown in Figure 9.

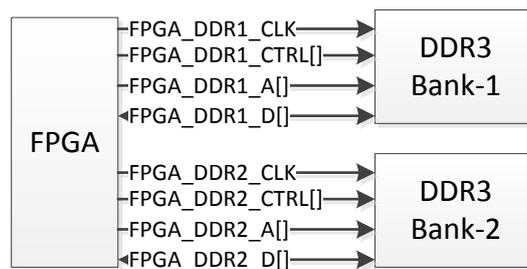


Figure 9: FPGA DDR3 memory banks

The VF360 Reference firmware connects the DDR3 memories to the ALTERA QSYS fabric, through which it can be access by the DSP via PCIe (core 0) or SRIO (cores 1-3).

2.5.4 QDR memories

The VF360 FPGA is connected to 16 MByte QDRII+ memory, arranged as two banks of 4M x 18-bit memory running at 400MHz (standard build). The two QDR banks are completely independent with separate clock, control address and data lines as is shown in Figure 10.

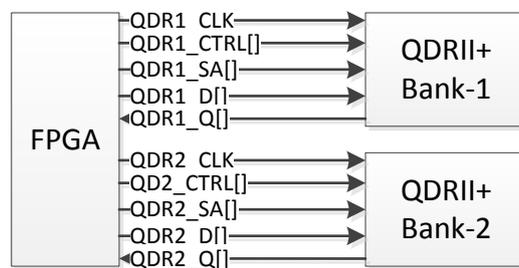


Figure 10: FPGA QDR memory banks

The VF360 Reference firmware connects the QDR memories to the ALTERA QSYS fabric, through which it can be access by the DSP via PCIe (core 0) or SRIO (cores 1-3).

2.5.5 FPGA High-Speed Serial Interfaces

The FPGA transceiver and reference clock connections are show in Figure 11. The left and right banks are swapped on the diagram, as it depicts the top view of the FPGA device.

The 18 right side transceivers connect to the User defined P2 VPX connector through X8d[4:1] and X12d[6:1] and to the FMC connector through FMC_DP[7:0]. Two of the reference clocks are provide by the FMC through GBTCLK[1:0]_M2C and one by the on-board Clock Generator through CLK_FPGA_Ref3 @ 125MHz.

Fourteen left side transceivers connect to the PCIe Switch through FPGA_PCl[e]7:0], to the DSP through SRIO[3:0] and to the FMC connector through FMC_DP[9:8]. CLK_FPGA_PCl[e] runs at 100MHz and Clk_FPGA_SRIO at 156.25MHz.

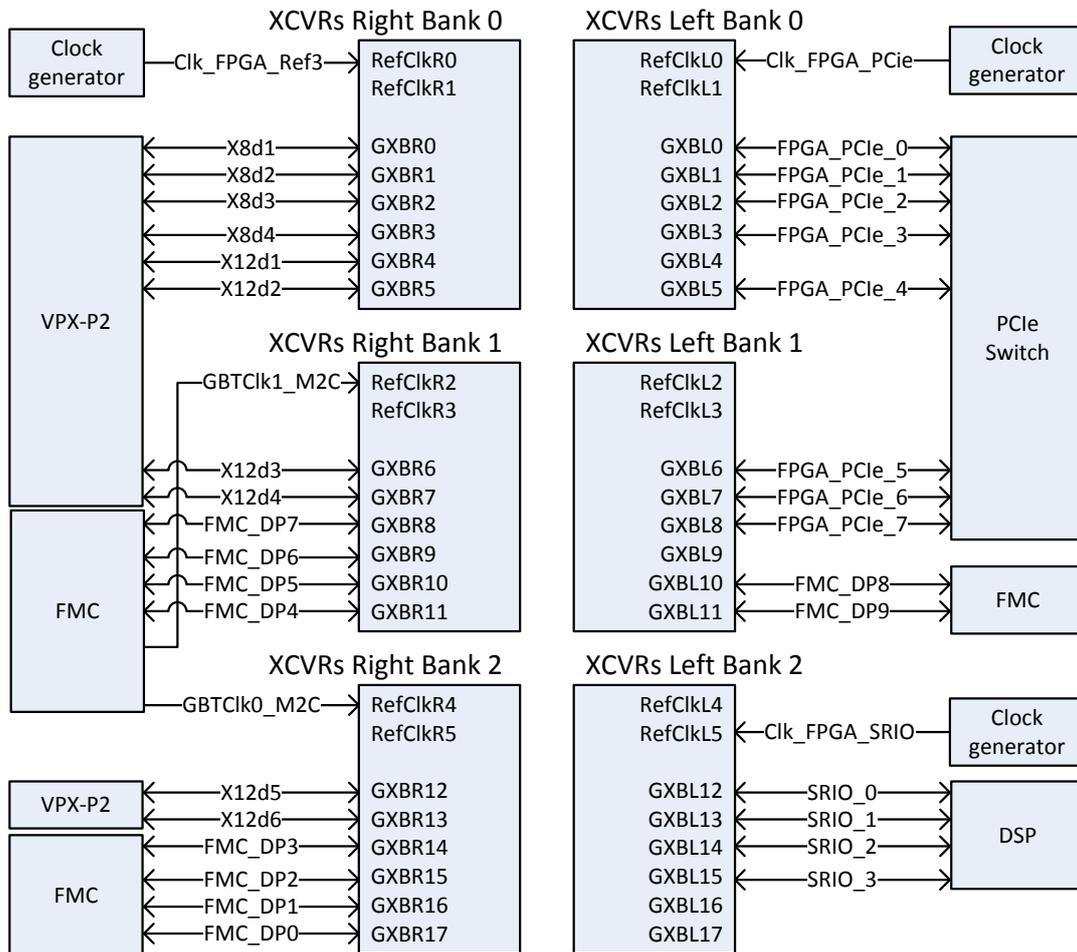


Figure 11: FPGA HSSI connections

2.6 VF360 Reset Structure

As described in § 2.2, nSYSRESET and local resets are performed by MANCON. MANCON generates the DSP and PCIe resets. The FPGA is reset by the DSP via GPIO0. A hard/warm or soft/cold reset can also be generated through **vf360mon**.

2.7 VF360 Clock Structure

The VF360 clock structure is show in Figure 12. The clock generator block generates the DSP Core, DDR, PCIe and SMII/SRIO clocks as well as the following FPGA clocks:

- CLK_FPGA_PClc[1:2]
- CLK_FPGA_SRIO
- CLK_FPGA_Ref (VPX REF_CLK)
- CLK_FPGA_Core (DDR & QDR memories)
- CKL_FPGA_125M
- CLK_FPGA_Ref3

Clock frequencies are listed in § 3 (Specifications). VPX REF_CLK (LVDS) is driven to or received from the backplane, depending on whether the VF360 is the system controller or not. Being a system controller, VPX REF_CLK can also be disabled through a BIOS option and then received from the backplane, refer to 6.1 for detail.

A CPLD divides a 25MHz clock input by two and routes a 12.5MHz clock to the FPGA.

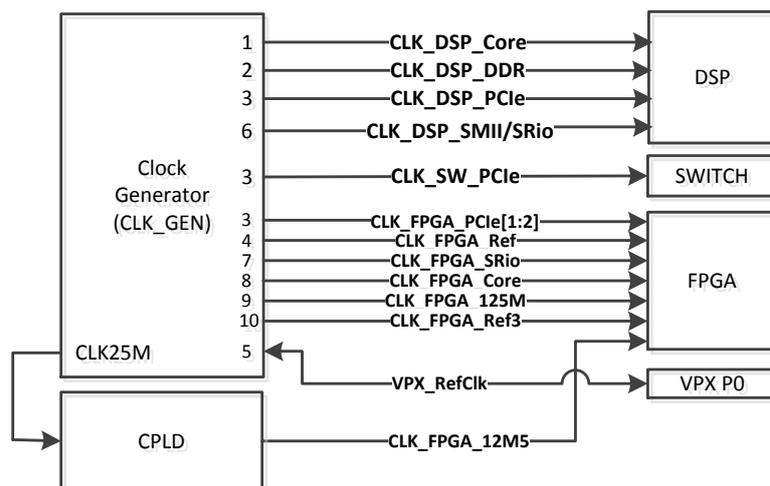


Figure 12: VF360 clock structure

The detail of the FPGA clocks and IO bank assignments are shown in Figure 13. Clock numbers are shown inside the PLL blocks of the diagram.

In the top side of the FPGA, the two QDR memories are placed in Bank 7 and the DDR memories in Bank 8. The top side is fed by the following generated clocks: FPGA_CLK_Core (100MHz), CLK_FPGA_PClE2 (100MHz) and CLK_FPGA_12M5.

In the bottom side of the FPGA, Bank 3 and Bank 4 (A-C) connect to the LA[0:33] and HA[0:23] differential signal pairs on the FMC connector, while the 24x single-ended VPX User IOs connect to Bank 4D.

The bottom side is fed by the following clocks: FPGA_CLK_125M, CLK_FPGA_Ref (25MHz) and P0_AUX_CLK. The FMC clocks Clk[0:1]_M2C and Clk[2:3]_BIDIR also connect to the bottom side. Clk[0:1]_M2C are parallel terminated at the FPGA. Clk[2:3]_BIDIR connect to FPGA clock inputs and to closely located FPLL clock outputs.

On the left side of the FPGA, CLK_FPGA_PClE (100MHz) connect to transceiver (XCVR) reference clock input REFCLK_L0 and Clk_FPGA_SRIO (156.25MHz) connect to REFCLK_L5.

The 8x PCIe lanes (connected to the PCIe Switch), the 4x SRIO lanes (connected to the DSP) and FMC_DP[8:9] (connected to the FMC site) connect to the transceiver interfaces on the left side of the FPGA.

On the right side of the FPGA, CLK_FPGA_Ref3 (125MHz) connect to transceiver (XCVR) reference clock input REFCLK_R0 and FMC clock outputs GBTCIk1_M2C and GBTCIk0_M2C to FPGA inputs REFCLK_R2 and REFCLK_R4 respectively.

The 4x VPX HSSI lanes (X8d[1:4]), the 6x VPX HSSI lanes (X12d[1:6]) and FMC_DP[7:0] (connected to the FMC site) connect to the transceiver interfaces on the right side of the FPGA.

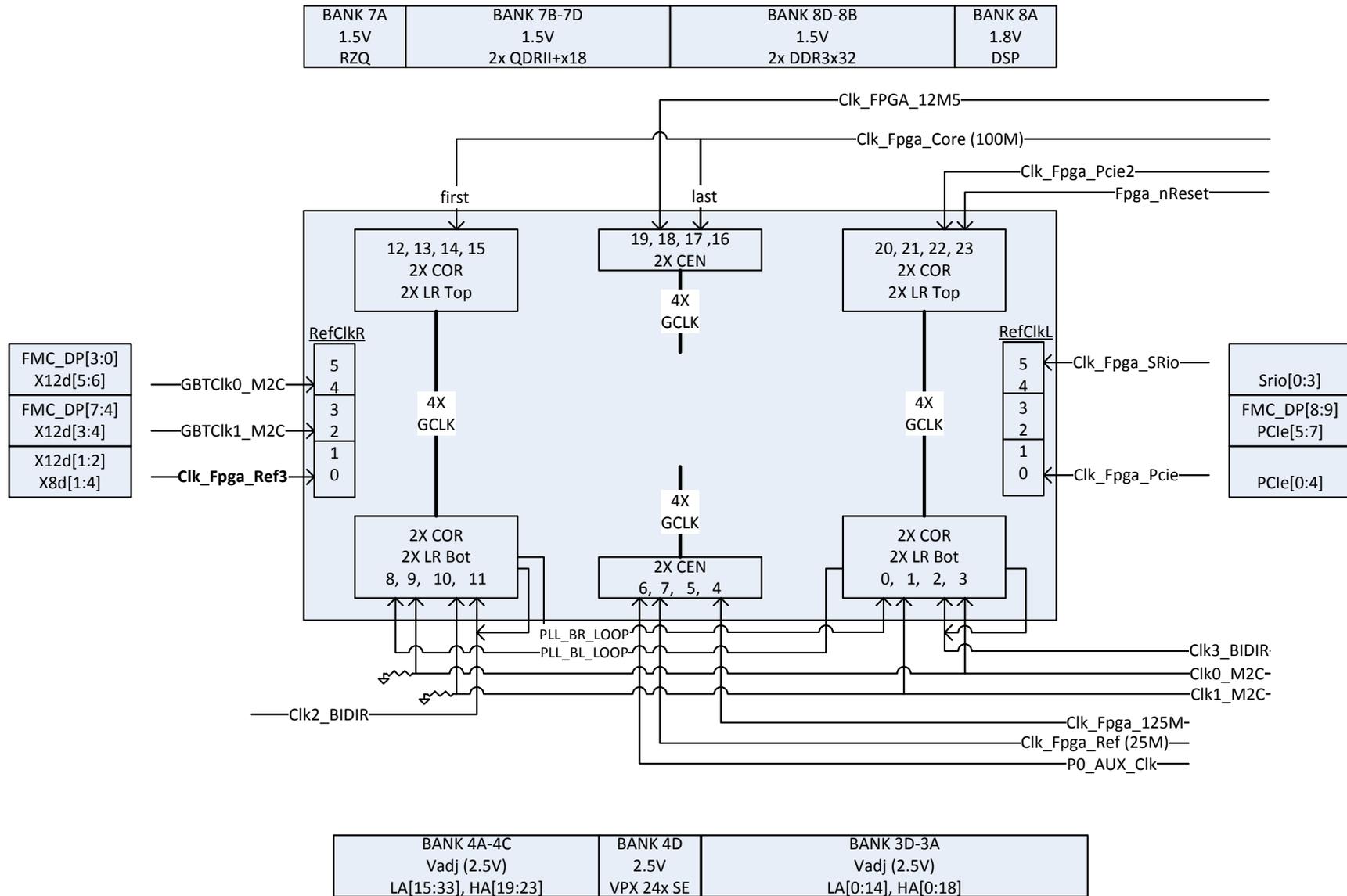


Figure 13: VF360 clocks and IO banks

2.8 Debug interfaces

The VF360 provides FPGA and DSP debug interfaces through the **VR300** Rear Transition Module (RTM) and the **FM500** FPGA Mezzanine Card (FMC). Both the VR300 and FM500 provide:

- ❖ XDS100v1 via DSP mini USB connector
 - Connect to TI TMS320C667X DSP
 - In Circuit Emulation (ICE)
 - USB Serial Port for debugging
 - Compatible with Code Composer Studio



Figure 14: FM500 FPGA Mezzanine Card

- ❖ USB-Blaster II via mini USB connector
 - Connects to Stratix® V FPGA
 - SignalTap® II Logic Analyzer
 - FPGA configuration and EPCQ Programming
- ❖ In addition to the above, the VR300 also provides a 1Gbps Ethernet connection from the DSP via a SFP cage.
- ❖ Jumper selection of DSP Boot option
- ❖ DSP reset push button

NOTE: Boot option and reset button **only** from issue-02 VR300 hardware



Figure 15: VR300 Rear Transition Module

3 Specifications

This chapter provides the specifications for the functional areas of the VF360.

3.1 General Specifications

1. OpenVPX MOD3-PAY-3F2U-16.2.12-2 module profile
2. VITA 57 FMC site with LA and HA connections
3. VPX P2 connections according to ANSI/VITA46.9 Pin Field **X24s+X8d+X12d**
4. FPGA Transceiver maximum speed:
 Transceiver Speed Grade 3... 8.5 Gbps
 Transceiver Speed Grade 2... 12.5 Gbps
5. DSP ↔ FPGA SRIO speed... 3.125Gbps

3.2 Environmental Specification

3.2.1 Temperature

Operating (AC2, FC2).....	-40 to 50 degrees Celsius with a linear air flow of > 2.5 m/s
Operating (CC2).....	-40 to 55 degrees Celsius at the thermal interface (high-end design)
Operating (CC3).....	-40 to 70 degrees Celsius at the thermal interface (typical design)
Non-Operating (C3).....	-50 to + 100 degrees Celsius

3.2.2 Vibration

Operating (V1).....	TBC
---------------------	-----

3.2.3 Dimensions

Size (PCB)	160 mm x 100 mm (excluding connectors)
Size (PCB)	171 mm x 100 mm (including connectors)
Weight (AC).....	450 g

3.3 Power Supply Requirements

The typical PSU currents required for the standard AC order code is shown in Table 2.

Table 2: VF360 Power supply requirements

PSU Rail	Nominal Voltage	Minimum Current & Power	Typical Current & Power	High Current & Power
Vs1	+12.0V	1A => 12W	1.5A => 18W	2A => 24W
Vs2	+3.3V	1.2A => 4W	1.2A => 4W	1.5A => 5W
Vs3	+5.0V	1.5A => 7.5W	2.4A => 12W	4A => 20W
3.3V_AUX	+3.3V	0.3A => 1W	0.3A => 1W	0.3A => 1W
Total Power		~ 25W	~ 35W	~ 50W

3.4 Ordering Information

The VF360 ordering information is shown below

Generic order code = VF360-A-B-C-D-E-F-G

- A: FPGA (A3, A4, A5, A7, A9, AB) for 5SGXA3, 5SGXA4, 5SGXA5, 5SGXA7, 5SGXA9 and 5SGXAB (D4, D5, D6, D8) for 5SGSD4, 5SGSD5, 5SGSD6 and 5SGSD8
- B: Speed grade (2 or 3) for Transceiver speed, (C or I) for Commercial/Industrial temp & (1 to 4) for FPGA speed
- C: DSP (1, 2, 4 or 8) for TMS320C667X one, two, four or eight DSP cores
- D: DDR3 (2 or 4) GB total DDR3 memory (1GB|2GB for FPGA + 1GB|2GB for DSP)
- E: QDRII+ (16 or 32) MB total QDRII+ memory (two banks of 8MB|16MB for FPGA)
- F: THERMAL (0 or 1) for air-cooled (AC) or conduction cooled (CC)
- G: Conformal Coating (0 or 1) for un-coated or coated

Standard AC order code = VF360-A3-3I4-4-2-16-0-0

5SGXA3 FPGA 3I4 speed grade (Industrial temperature)
 TMS320C6674 four core DSP @ 1GHz
 DDR3 = 2GB, 1GB for FPGA (2x 512MB) + 1GB for DSP
 QDRII+ = 16MB (2x 8MB) for FPGA
 Air-cooled, un-coated

8-core DSP AC order code = VF360-A3-3I4-8-2-16-0-0

5SGXA3 FPGA 3I4 speed grade (Industrial temperature)
 TMS320C6678 eight core DSP @ 1.25GHz
 DDR3 = 2GB, 1GB for FPGA (2x 512MB) + 1GB for DSP
 QDRII+ = 16MB (2x 8MB) for FPGA
 Air-cooled, un-coated

Standard CC order code = VF360-A3-3I4-4-2-16-1-1

5SGXA3 FPGA 3I4 speed grade (Industrial temperature)
 TMS320C6674 four core DSP @ 1GHz
 DDR3 = 2GB, 1GB for FPGA (2x 512MB) + 1GB for DSP
 QDRII+ = 16MB (2x 8MB) for FPGA
 Conduction Cooled, coated

Contact factory for other order options

4 Installation and Setup

This chapter includes instructions for unpacking and installing the VF360.

4.1 Unpacking the product



Before unpacking the product, note the following guidelines:

1. Check the shipping carton for damage. If the product's shipping carton is damaged upon arrival, request that the carrier's agent be present during unpacking and inspection of the board.
2. Once unpacked, the board should be inspected carefully for physical damage, loose components etc. In the event of the board arriving at the customer's premises in an obviously damaged condition, Parsec or its authorized agent should be notified immediately.
3. Make sure that the area designated for unpacking the product is a static electricity controlled environment. Unpack the VF360 board *only* on a ground conductive pad using an anti-static wrist strap grounded to the pad.
4. If moving the board is necessary, move it in an ESD protective container.
Note: The VF360 board is shipped in an ESD protective container.

4.2 Installing the VF360 Hardware

Once the VF360 has been unpacked and inspected, it can be installed in a 3U VPX slot that is compatible with module profile MOD3-PAY-3F2U-16.2.12-1/2 and the following slot profiles:

- ❖ SLT3-PAY-3F2U-14.2.13
- ❖ SLT3-PAY-2F2U-14.2.3
- ❖ SLT3-PAY-1F2U-14.2.12



Plugging the VF360 into any other slots is NOT supported and can seriously damage the VF360. Parsec should be contacted on any questions regarding VF360 compatible VPX slots.



It is strongly advised that, when handling the VF360 and its associated components, the user should wear an earth strap to prevent damage to the board as a result of electrostatic discharge.

The board is installed and powered up as follows:

- ❖ Attach an antistatic wrist strap to your wrist. Attach the other end to ground.
- ❖ Power down the VPX rack.
- ❖ Inspect the VF360 VPX connectors for any damage or debris.
 ✓ DO NOT insert the VF360 if any connector damage or debris is visible.
- ❖ Carefully insert the VF360 into the VPX slot and secure by using the front panel handle.
- ❖ Secure the front panel with mounting screws at the top and the bottom.
- ❖ Apply power to the VPX rack and observe the LEDs through the small front panel holes
 - The top LED should flash yellow, indicating the Linux heartbeat.
 - The 3rd LED from the top should flash green (@ 2Hz) indicating that the FPGA clock is running.

4.3 Installing the VF360 Software and Firmware

The CD shipped with the VF360 contains the following:

- ❖ **Documentation**
- ❖ **Software (BSP)**
 - Linux kernel, Linux file system and IBL
 - Linux PCIe driver (PCI-04) and test application for FPGA PCIe interface
 - Linux PCIe Endpoint drivers (EP) and Root Complex (RC) drivers for DSP
 - Linux X86 drivers for DSP and FPGA.
 - SYS/BIOS sample application for SRIO communication between DSP and FPGA

No files from the CD need to be transferred to the VF360.

The PCI-04 and SBC drivers need to be installed on an X86 based Single Board Computer (SBC) performing the System Controller function, with a VF360 as a Slave module (non-System Controller) in the VPX rack. Refer to [1] for more detail on the VF360 software BSP and Endpoint mode.

- ❖ **Firmware**

The VF360 FPGA is configured with the Firmware Reference Design after power-up, no firmware need to be installed onto the VF360. Refer to [2] for more detail on the VF360 Firmware Reference Design.

4.3.1 Directory structure

The VF360 CD directory structure shown in Table 3.

Table 3: Install CD directory structure

Directory	Description\ Contents
\Documents	VF360 User Manual VF360 Software Reference Manual VF360 Firmware Reference Manual FM500 FMC Product Brief VR300 RTM Product Brief
\Software\binaries	Linux kernel, Linux filesystem and IBL (Bootloader) binaries
\Software\kernel	Linux kernel source code and build files
\Software\pci04	Linux PCI04 driver and test application for FPGA PCIe interface
\Software\pci_ep	Root DIR for endpoint drivers
\Software\pci_ep\ep_drv	Linux PCIe driver for DSP EP (endpoint) on VF360 Slave module
\Software\pci_ep\vf360_drv	Linux PCIe driver and test application for DSP RC (Root complex) on VF360 System Controller module
\Software\pci_ep\sbc_drv	Linux PCIe driver and test application for X86 SBC RC
\Software\sys_bios	SYS/BIOS sample application for SRIO communication between DSP and FPGA
\Firmware	Root DIR for firmware files

4.4 Installing Code Composer

Code composer Version 5.3 needs to be installed as development/debug environment for VF360 software. This also installs the drivers for the XDS100 emulator on the FM500 FMC and VR300 RTM.

4.5 Installing Quartus II

Quartus II Version 14.0 or later needs to be installed as development/debug environment for VF360 firmware. This also installs the drivers for the USB-Blaster II on the FM500 FMC and VR300 RTM.

4.6 Installing a terminal program

A terminal program like Windows Hyper Terminal or PuTTY need to be installed, since the VF360 does not have a GUI.

PuTTY can be found at www.putty.org

The VF360 is now ready for use, refer to § 5 for more detail.

5 Operating Guide

This chapter provides information on proper operation of the VF360.

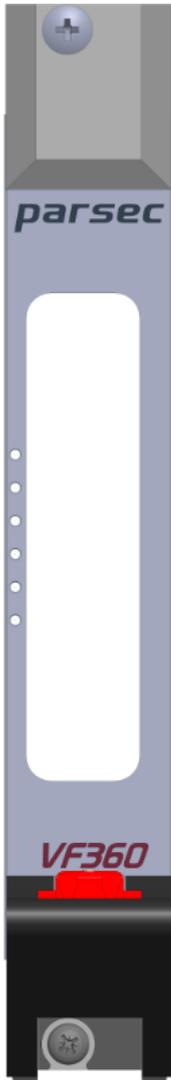
5.1 Configuration Settings

All configuration settings on the VF360 are performed through the BIOS settings, refer to § 6.1 for detail.

5.2 Status Indicators

The VF360 has six front panel LEDs mounted on the bottom side of the PCB, visible through small pinholes in the front panel. The top two yellow LEDs are connected to the DSP and the bottom four LEDs to the FPGA. The LED functions allocated to the DSP and the Firmware Reference Design is shown in Table 4.

Table 4: Front panel LED indicators



Position	LED	Status	Status description
1 st LED yellow (top)	D18	Flashing	Linux heartbeat
2 nd LED yellow	D17	Flashing	Linux NAND flash access (HDD)
3 rd LED green	D16	Flashing at 2Hz	FPGA out of reset and CLK_FPGA_125M is running
4 th LED green	D15	Flashing at 0.5Hz	FPGA QDR initialized
5 th LED green	D14	Flashing at 0.5Hz	FPGA DDR initialized
6 th LED green (bottom)	D13	On	FPGA SRIO initialised

5.3 VF360 Software

This section describes aspects related to software development on the VF360. The VF360 boots Linux on DSP core0 and runs SYS/ BIOS on the remaining cores. For detail on the BSP, refer to [1].

5.3.1 DSP PCIe mode (Root Complex or Endpoint)

When the VF360 is booted in the System Controller (SYS_CON) slot of the VPX rack, the DSP is the Root Complex of the PCIe bus and enumerates all PCIe endpoints.

When the VF360 is **not** in the System Controller (SYS_CON) slot of the VPX rack, the DSP can act as a PCIe Endpoint ('Slave') and be enumerated by the System Controller (typically a Single Board Computer). For the DSP to function as a PCIe Endpoint, the *PCI Endpoint* setting must be enabled in the VF360 BIOS, as the default is *Off*.

It may be necessary to delay the PCIe enumeration of the SBC until the VF360 DSP has booted. This can be done in one of two ways:

1. Change the PCIe reset delay in the BIOS of the SBC to > 15s.
2. Enable the open-collector SYSRESET output of the VF360 (as a Slave module) in the VF360 BIOS. This causes the VF360 to keep the System Controller SBC in reset until the VF360 DSP has booted. The DSP Endpoint will then be enumerated by the SBC. Refer to § 6.1 for detail on the VF360 BIOS options.

5.3.2 XDS100 serial port

Plug a USB cable into the mini USB connector labelled DSP on the FM500 or VR300. Refer to § 2.8 for detail.

To connect to the DSP serial port, set-up PuTTY (or other terminal emulator) to 115200 baud, 8N1 with no flow control. When powering the VF360 while connected to PuTTY, the Linux booting information should be displayed in the terminal window.

Type **ifconfig**; the VF360 IP address should be displayed if connected to a DHCP server.

```
/ # ifconfig
eth0      Link encap:Ethernet  HWaddr 00:17:EA:D4:A1:15
          inet addr:172.17.7.58  Bcast:172.17.255.255  Mask:255.255.0.0
          UP BROADCAST RUNNING MULTICAST  MTU:1500  Metric:1
          RX packets:105 errors:0 dropped:0 overruns:0 frame:0
          TX packets:18 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:11033 (10.7 KiB)  TX bytes:5808 (5.6 KiB)
          Interrupt:48

lo        Link encap:Local Loopback
          inet addr:127.0.0.1  Mask:255.0.0.0
          UP LOOPBACK RUNNING  MTU:16436  Metric:1
          RX packets:0 errors:0 dropped:0 overruns:0 frame:0
          TX packets:0 errors:0 dropped:0 overruns:0 carrier:0
          collisions:0 txqueuelen:0
          RX bytes:0 (0.0 B)  TX bytes:0 (0.0 B)
```

Figure 16: **ifconfig** terminal window

The VF360 default setup is for a dynamic IP address by a DHCP server. This can be changed to a static IP by editing `rc.sysinit` in `/etc`. Remove comment (`#`) before the `ifconfig` command and comment out the `udhcpc`

```
command. #ifconfig eth0 10.0.20.32
udhcpc
```

Type `lspci`; as a minimum the VF360 PLX PCIe Switch and the ALTERA FPGA should be displayed.

```
/ # lspci
00:00.0 PCI bridge: Texas Instruments Device b005 (rev 01)
01:00.0 PCI bridge: PLX Technology, Inc. PEX 8624 24-lane, 6-Port PCI Express Gen 2 (5.0 GT/s) Switch [ExpressLane] (rev bb)
02:00.0 PCI bridge: PLX Technology, Inc. PEX 8624 24-lane, 6-Port PCI Express Gen 2 (5.0 GT/s) Switch [ExpressLane] (rev bb)
02:01.0 PCI bridge: PLX Technology, Inc. PEX 8624 24-lane, 6-Port PCI Express Gen 2 (5.0 GT/s) Switch [ExpressLane] (rev bb)
02:04.0 PCI bridge: PLX Technology, Inc. PEX 8624 24-lane, 6-Port PCI Express Gen 2 (5.0 GT/s) Switch [ExpressLane] (rev bb)
02:05.0 PCI bridge: PLX Technology, Inc. PEX 8624 24-lane, 6-Port PCI Express Gen 2 (5.0 GT/s) Switch [ExpressLane] (rev bb)
02:08.0 PCI bridge: PLX Technology, Inc. PEX 8624 24-lane, 6-Port PCI Express Gen 2 (5.0 GT/s) Switch [ExpressLane] (rev bb)
06:00.0 Unassigned class [ff00]: Altera Corporation Device e001 (rev 01)
/ #
```

Figure 17: `lspci` terminal window

5.3.3 Ethernet connection

Connect an Ethernet cable into SFP transceiver module on the **VR300**, or into the Ethernet Switch card in the VPX rack. Telnet to the VF360 on port 23 and login as root. The terminal should now show the Linux root directory.

5.3.4 Monitor application and BIOS settings

The Linux host (running on DSP Core0) runs a **VF360 Monitor application** (`vf360mon`) that serves important **VF360** related information via Ethernet. The `vf360mon` help screen is shown in Figure 18.

For more detail on `vf360mon`, refer to § 6.1.

For more detail on the VF360 BIOS options, refer to § 6.2.

```
ping      [ip]                Check if host is alive [optionally return IP address]
rtc       [set y m d h m s]   Get or set RTC
time      Get VF360 local time
status    [adc/temp/rail/pll/  Get status of VF360
          raw/syscon]
hwinfo    [ser/hw/dsp/fpga]   Get hardware information
osinfo    Get Linux OS information
version   [mon/mancon/reflex/pci] Get version of component[s]
bit        [mon]             Get BIT of VF360
bios      Show bios settings
          [reset user/safe]   Reset user or safe bios defaults
          [u reg val1 [val2]] Update user bios register with new values
          [help reg]         Show valid register settings
log        Show log entries
          [clear pass]       Clear log
reset      [0/1]             Reset DSP/VF360
          [soft/hard]
          [warm/cold]
reboot    Reboot DSP (alias for reset 0)
restart   Restart VF360 (alias for reset 1)
pass      password           Authenticate connection to access protected commands
```

Figure 18: `VF360mon` help screen

5.3.5 FPGA Configuration

The FPGA can be configured from a Raw Binary File (RBF) by the DSP (under Linux) with the following procedure:

`“cd /fpga”`

`“./fpgaprogram.sh <RBF file name>”`

5.3.6 Code Composer

Run Code Composer (Version 5.3 or later). Create a new Target Configuration under View => Target Configurations => Create New target Configuration File

Select the **XDS100v1** connection and the **TMS320C6674** device.

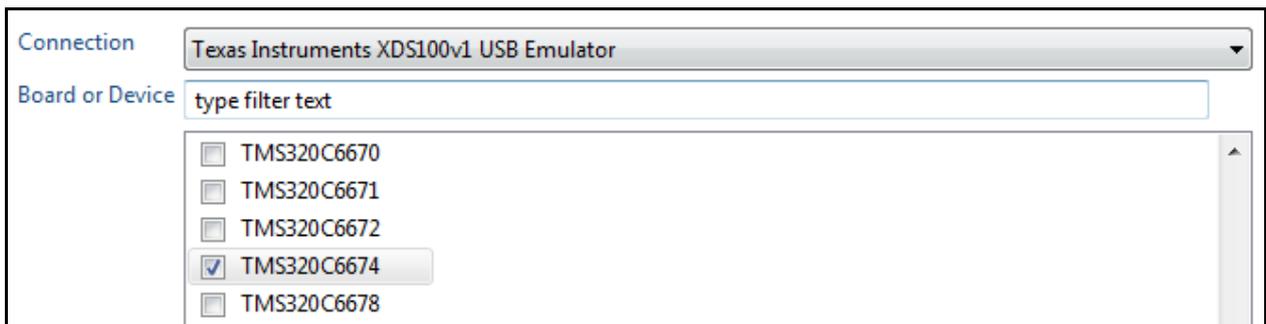


Figure 19: Code Composer target Configuration

Save the configuration and Test the connection, it should pass.

Go to View => Target Configurations and **Launch** the **Selected Configuration** (right click). It should now display the four DSP cores. Right click on a Core (C66xx_0/1/2/3) and **Connect**.

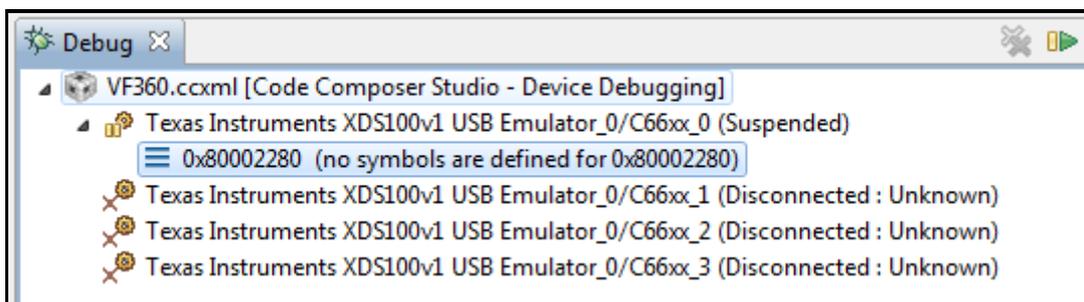


Figure 20: Code Composer DSP Core0 connected

A compiled .out file can now be loaded onto a DSP core with the Run => Load Program command

5.3.7 DSP Boot options

The VF360 provides a dual-boot option for the DSP from NAND flash.

This allows the VF360 to boot from other operating systems which are typically used for:

- Real-time control
- DSP processing
- Safety critical applications

For solutions requiring other operating systems for deployment, the VF360 can be booted from the 2nd OS partition (OS2), or OS1 can be overwritten with the required operating system. A recovery boot partition is provided in-case the default boot partition is corrupted. The NAND flash has 8 partitions as is shown in Table 5 and contains Operating System (OS) and File System (FS) partitions.

With the default BIOS settings, the DSP boots Linux from OS1 and uses the file system in FS1.

Table 5: NAND flash partitions

Partition	Size (MB)	Name	Description	Default contents
0	0.25	Reserved	N/A	Empty
1	15.75	OS1	Default boot OS	Linux kernel
2	240	FS1	Default FS	Linux file system
3	16	OS2	2 nd boot OS	Empty
4	256	FS2	2 nd FS	Empty
5	432	FS3	3 rd FS	Empty
6	8	Recovery OS	Recovery OS	Linux kernel
7	56	Recovery FS	Recovery FS	Linux file system

The boot selection can be made through the Boot BIOS setting, or through the GDiscrete1 OpenVPX backplane signal, refer to § 6.2 for detail.

When the GDiscrete1 BIOS Boot option is selected, the level of GDiscrete1 at boot time determines which OS is booted from. When a VR300 Test RTM is present in a system, GDiscrete1 can be controlled by the J2 jumper on the VR300, refer to Table 6.

Table 6: GDiscrete1 Boot selection

GDiscrete1 level	Boot OS	Boot FS	VR300 J2 jumper position
Low	OS1	FS1	Position 2-3
High	OS2	FS2	Position 1-2 (or open)

An example SYS/BIOS application binary that can be booted from is provided on the default Linux file system, refer to for [1] detail.

5.3.8 SYS/BIOS development

On the VF360 CD, as part of the BSP, there is a Code Composer project that runs under SYS/BIOS. This example application shows how the FPGA is accessed by the DSP via the SRIO interface.

5.3.9 Linux development

Information on the TI DSP Linux kernel and development compilers, refer to <http://linux-c6x.org>

5.4 VF360 Firmware

A block diagram of the VF360 Firmware Reference Design is shown in Figure 21 and contains the following main blocks; VF360_dsp_if, VF360_mem_if, HSSI and User_logic.

The **vf360_dsp_if** block provides the PCIe and SRIO external interfaces, as well as Avalon Streaming (AST) and Avalon Memory Mapped (AMM) internal interfaces to **vf360_mem_if** and **user_logic**.

The **vf360_mem_if** block provides the external interfaces for the two DDR3 and two QDRII+ memory banks, as well as the AMM internal interfaces to access them via PCIe or SRIO.

The **hssi** block provides transceiver interfaces for the 18 HSSI links on the right bank of the FPGA. These transceivers can be setup and controlled (by the DSP) via the HSSI AMM control bus.

The **user_logic** block is a template for users to implement their own firmware.

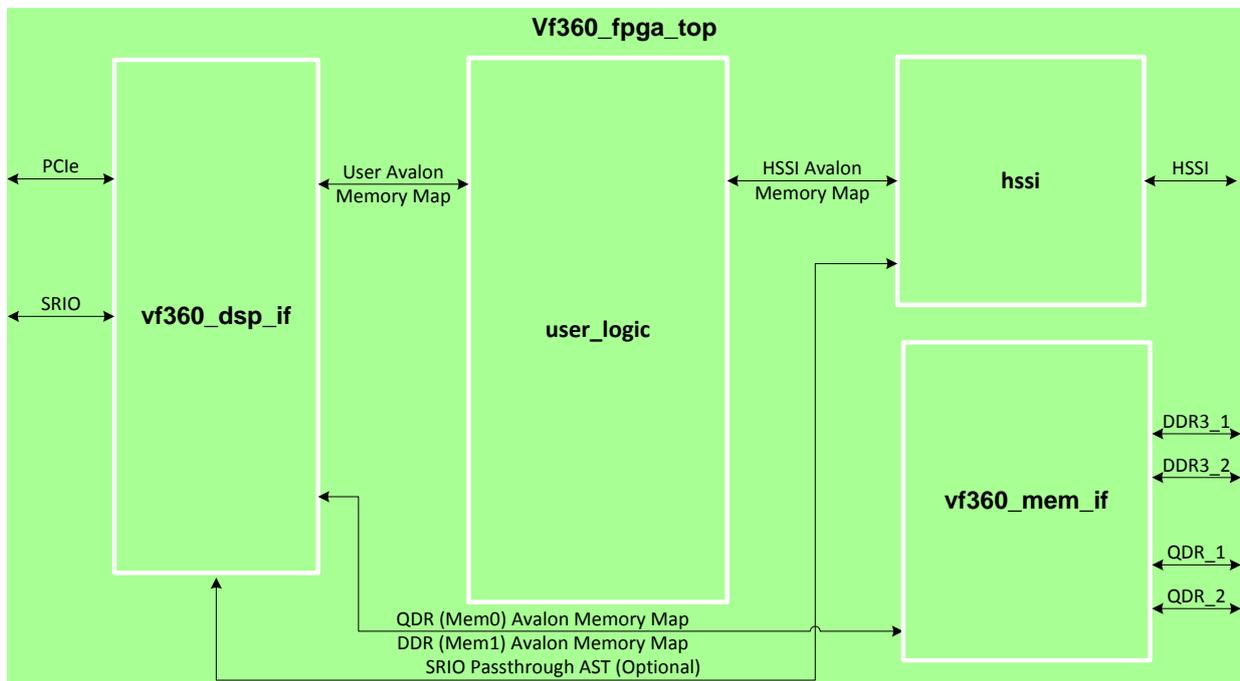


Figure 21: VF360 Firmware Reference Design top level diagram

For more detail on the VF360 firmware, refer to the VF360 Firmware Reference Manual [2].

5.4.1 FPGA BAR Requirements

Table 7 gives an overview of the VF360 FPGA PCIe BAR requirement. For more detail refer to [2].

Table 7: Overview of FPGA PCIe BAR requirement

Memory space	Size requested
PCIe BAR0	16MB
PCIe BAR1	256KB
PCIe BAR2	32KB

5.4.2 ALTERA USB-Blaster II

Plug a USB cable into the mini USB connector labelled FPGA on the FM500 or VR300. Refer to § 2.8 for detail.

NOTE: On the VR300 the FPGA mini USB connector is close to the VPX backplane connectors and is accessed through the slot in the PCB.

When prompted for the USB-Blaster driver, browse to the “\altera\quartus\drivers” directory for completion of the installation.

Run the Quartus II Programmer, click on “Hardware Setup” and select the available USB-Blaster.

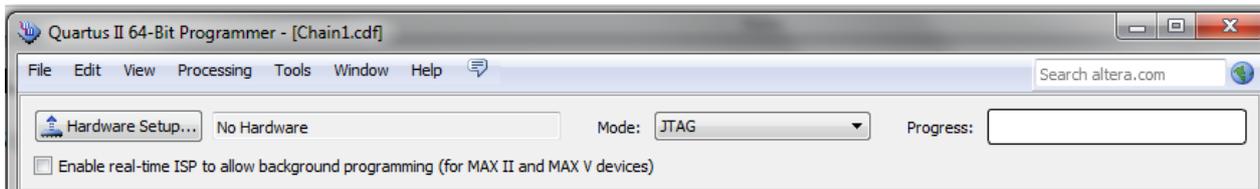


Figure 22: ALTERA USB-Blaster setup

5.4.3 Configuring the FPGA

To configure the FPGA (volatile), click on “Auto Detect” and select the relevant FPGA device, i.e. 5SGXMA3K3 for the standard VF360. The FPGA is now listed. Right click on the FPGA in the list, select “Change File” and browse to the .SOF file to configure the FPGA with. Tick the “Program/Configure” box and press “Start”. The VF360 FPGA will now be configured with the selected .SOF file.

The FPGA configuration is volatile and will be lost after a power cycle.

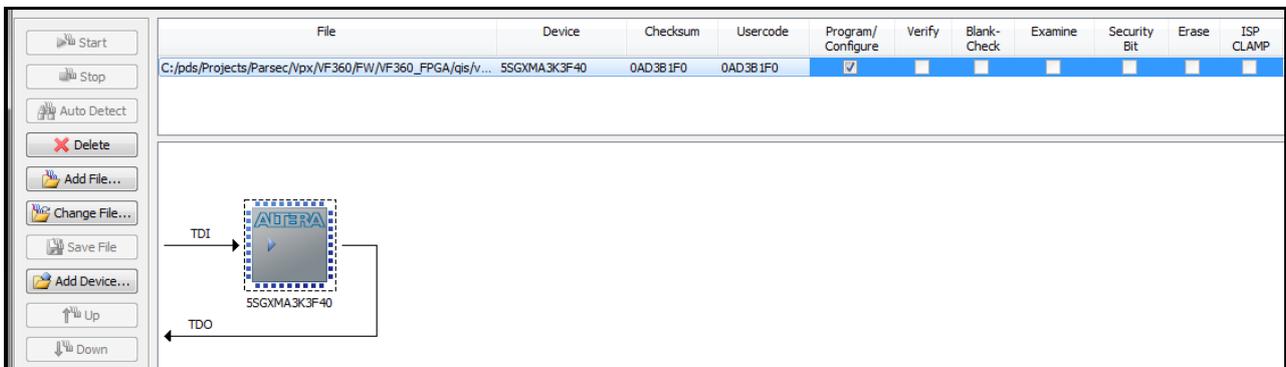


Figure 23: FPGA configuration via JTAG

5.4.4 Programming the FPGA configuration device

To program the FPGA configuration device (EPCQ), a .JIC file first need to be created from the .SOF file.

In Quartus II or the Quartus II Programming, go “File => Convert Programming Files”

- Set **Programming File Type** to => .JIC
- Set **Configuration Device** to => EPCQ256
- Set **Mode** to => Active Serial x4

Select **Flash Loader** and click on **Add Device**, select the **Stratix V** Device family and the **5SGXMA3K3** Device name (standard VF360).

Select **SOF Data** and then **Add File** to add the SOF file created in Quartus, refer to [2] for detail.

Select the added SOF file, click on **Properties** and tick (enable) the **Compression** box, then press **OK**

Click **Generate** to create the .JIC file

Add the generated JIC file to the Quartus II Programmer and program the FPGA.

Power cycle the VF360 and the FPGA will be configured with the programmed SOF data.

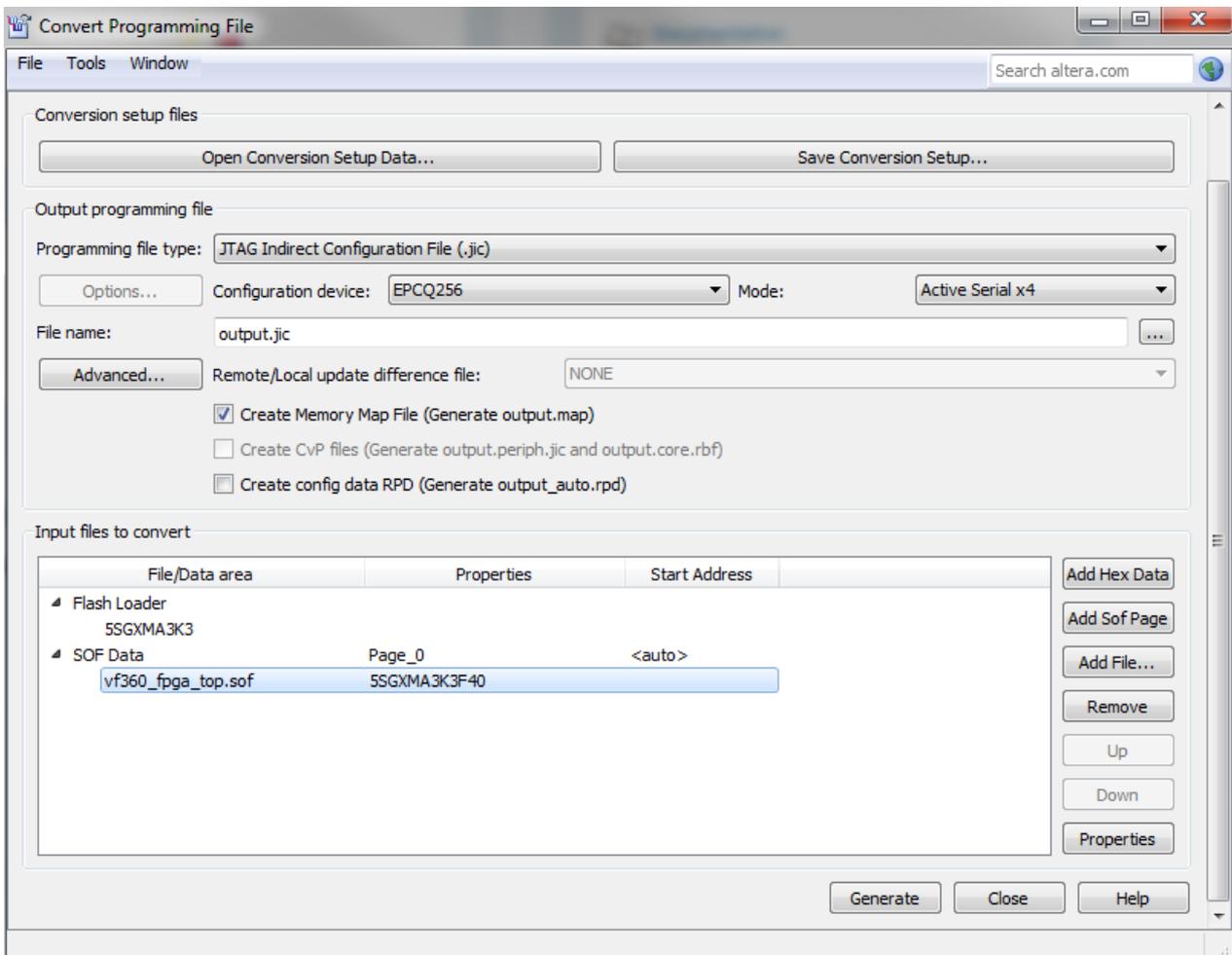


Figure 24: FPGA programming via JTAG

6 Monitor, BIOS & GPIOs

This chapter describes the VF360 BIOS settings and the DSP GPIO usage.

6.1 Monitor commands

Vf360mon is accessed via telnet port 4360, i.e. *telnet <IP> 4360*. When using the XDS100 serial port on the FM500 FMC or VR300 RTM, **vf360mon** is access by *telnet 127.0.0.1 4360*.

The vf360mon commands are listed in Table 8

Table 8: VF360mon commands

Command	Description
help	List the vf360mon commands
ping	Check if host replies with a pong
rtc	Get or Set the real-time clock on the VF360
time	Shows the time of the Linux OS
status	Shows status of PSU rails, device temperatures and clock generator
hwinfo	Shows hardware status (i.e. Serial number, PCB, Mechanics, DSP, FPGA and memories)
osinfo	Shows Linux uptime, RAM usage and loading
version	Shows the versions of vf360mon, MANCON SW and FPGA FW
bit	Check vf360mon communication between DSP and MANCON
bios	Shows the safe default and user BIOS settings
log	Shows boot or PSU failures
reset	Performs a warm or cold reset of the VF360. A warm reset, resets the DSP A cold reset re-powers the VF360
reboot	Same a warm reset
restart	Same as cold reset
pass	Unlocks the protected command, i.e. BIOS reset and update

6.2 BIOS settings

The VF360 provide a set of **user** BIOS settings and a **safe** default set. The BIOS is accessed through the **vf360mon** service that is accessed via *telnet <IP> port 4360*. The user settings can be reset back to the safe defaults by entering **reset user** in the BIOS menu.

To access the BIOS settings a password is required; type "*pass vf360*".

A BIOS command is executed by typing "*bios command parameters*"

The BIOS commands provided are listed in Table 9.

The VF360 can be forced to boot with the following safe default BIOS values:
Ethernet_auto_neg, LinuxMem and PCIe_EP.

This is done by pressing "s" on DSP serial port terminal while re-booting Linux.

Table 9: BIOS Commands

Command	Parameter(s)	Description
bios		List the safe default and user BIOS Register values
reset	user / safe	Resets the user BIOS settings back to the safe settings Resets the safe BIOS settings back to hardcoded safe settings
u	Register Val1 [Val2]	Updates a BIOS register with value specified in Val1. Some registers requires 2 parameters, Val1 and Val2
help	Register	Provides help on a specific BIOS register

Table 10 gives an overview of the VF360 BIOS settings. For the most current BIOS settings and options, run the **bios** command in **vf360mon**. Run **help <entry>** for detail on a specific entry.

Table 10: BIOS Register Settings

BIOS Register Entry	Default	Description
System_Controller	Backplane	Sets VF360 System_Controller mode to On, Off or Backplane determined.
SYSRESET	System_Controller	Sets SYSRESET output as On or System Controller
SYSRESET_Delay	0	Additional SYSReset delay in 250ms increments
PCleRESET_Delay	0	Additional PCle Reset delay in 250ms increments
MaskableReset_Input	Off	Enable Maskable Reset for DSP warm reset (from RTM or FMC)
NVMRO	Off, non-active	Non-Volatile Memory Read Only enable and activate
System_Management	Off	Enable System Management bus SM[3:0]
Ethernet_auto_neg	ETH0 = On ETH1 = Off	Set DSP Ethernet auto negotiate mode on ETH1 (CPUTP02) and ETH0 (CPUTP01).
Fixed_Vadj	2.5V (BIOS)	Set Vadj voltage from BIOS or FMC
LinuxMem	896 MB	Memory allocated to Linux running on 1 st core (Core0)
PCle_BKP	On, On, On	Enable/Disable Backplane PCle ports DP01, DP02 & DP03
PCle_EP	Off, 32MB	Activate Slave mode DSP PCle endpoint (EP) and set EP BAR size
Boot	Boots OS1 & FS1	Selects the Boot Operating System (OS) and File System (FS). Refer to § 5.3.7.
CLK_DSP_Core	Reserved	
CLK_DSP_DDR	Reserved	
CLK_PClE	Reserved	
CLK_FPGA_Ref	Reserved	
REF_CLK	System_Controller @ 25 MHz	VPX P0 RefClk output set as Off or System_Controller @ frequency
CLK_DSP_SRIO	Reserved	
CLK_FPGA_SRIO	Reserved	
CLK_FPGA_Core	Reserved	
CLK_FPGA_125M	Reserved	
CLK_FPGA_Ref3	125MHz	Frequency of CLK_FPGA_Ref3

BIOS Register Entry	Default	Description
DSP_ClockSpeed	Auto	Selects the clock speed of the DSP cores.

6.3 GPIOs

The DSP GPIOs are used to determine the DSP boot mode during start-up. After DSP booting some of the GPIOs are available to the user for specific (fixed) or general purpose (user defined) functions, e.g. communication between the DSP and the FPGA. Some GPIOs are *reserved* for board management functions.

Table 11 lists the DSP GPIOs and indicates which are available to the user.

Table 11: DSP GPIOs

GPIO	FPGA Connection	Function
0	Yes	Fixed: FPGA Reset (active low)
1	Yes	User defined
2	Yes	User defined
3	Yes	User defined
4	Yes	Fixed: P1_Gdiscrete input from P1
5	Yes	Fixed: P1_Gdiscrete output to P1
6	Yes	<i>Reserved: FPGA_nStatus input to DSP</i>
7	Yes	<i>Reserved: FPGA_ConfDone to DSP</i>
8	Yes	<i>Reserved: 1PPS RTC_MFP (IRQ) to DSP</i>
9	Yes	<i>Reserved: TBD</i>
10	Yes	<i>Reserved: Linux Heartbeat LED</i>
11	Yes	User Defined
12	Yes	User Defined
13	Yes	<i>Reserved: Linux NAND activity LED</i>
14	No	<i>Reserved: FPGA nConfig</i>
15	No	<i>Reserved: FPGA Configuration Enable</i>

7 Acronym List

AC	Air cooled
BAR	Base Address Register
BSP	Board Support Package
CC	Conduction Cooled
DMA	Direct Memory Access
DSP	Digital Signal Processor
EP	Endpoint
ESD	Electrostatic Discharge
EW	Electronic Warfare
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
FS	File System
HSSI	High-Speed Serial Interface (FPGA transceivers)
JTAG	Joint Test Action Group
KB	Kilo Byte(s)
MB	Mega Byte(s)
Mb	Mega Bit(s)
MT/s	Mega Transfers per second
MSPS	Mega Samples Per Second
OS	Operating System
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCIe	PCI Express
PLL	Phase Locked Loop

PSU	Power supply
RBF	Raw Binary File
RC	Root complex
RTM	Rear Transition Module
SEEP	Serial EEPROM
SDR	Software Defined Radio
SFP	Small form-factor pluggable
SIGINT	Signals Intelligence
SRIO	Serial Rapid IO

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