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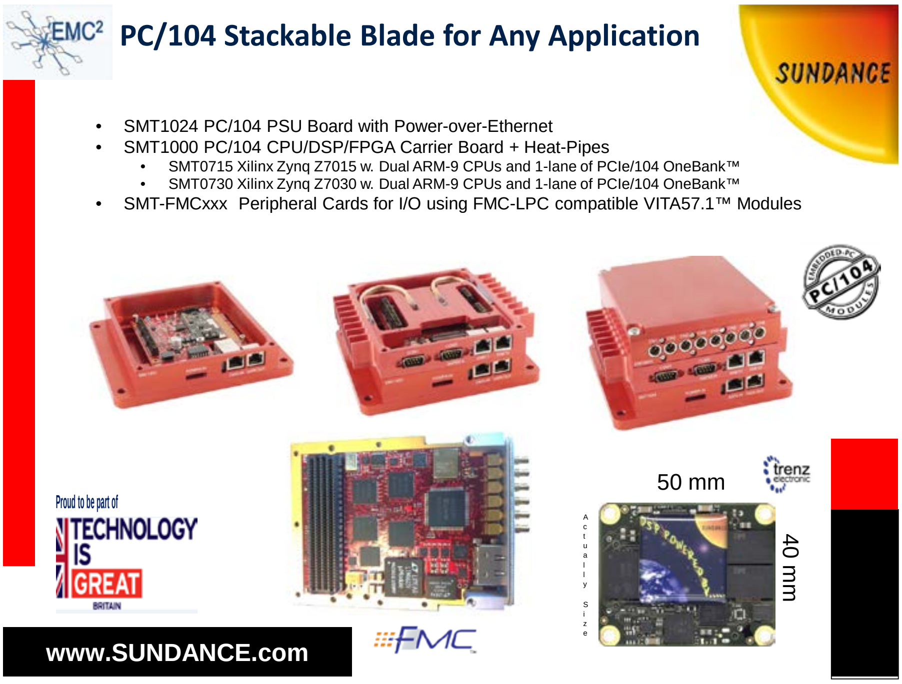
EMC²-DP

PCIe/104 OneBank™ Carrier for ARM CPU + FPGA + VITA57.1 FMC™ Modules



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Revision History

Issue	Changes Made	Date	Initials
1.0	First draft.	25/10/13	GKP
2.0	Major update	17/9/14	GKP
2.0.1	Cosmetics	28/10/14	FC
2.0.2	Updated board layout.	5/11/14	GKP
2.0.3	Removed USB interface on PCIe104 connector. Added MIO detail. Added MEMS (accelerometer) on main board.	23/1/15	GKP
2.1.0	Added PCIe switch	6/3/15	GKP
2.2.0	Added new Visio drawings and photos	17/03/15	FC
2.2.1	Added detail to PCIe switch	1/4/15	GKP

Table of Contents

1 Introduction

This document describes the hardware features and some operational details of how the EMC²-DP will become a PCIe/104 OneBank™ Board with Dual ARM9 CPU + Re-configurable FPGA Logic and interface to CPU specific I/O features and how the EMC²-DP can be used as either a Host Controller in a PC/104 Stack or as stand-alone.

Some discussion is made of how these features can be implemented with specific devices and how EMC²-DP can be expanded with a VITA57.1 FMC® compatible Daughter Cards for I/O expansion from the FPGA fabric.

1.1 Main Features

1.1.1 Hardware

This board consists of the following major hardware features:

1) Based on the Xilinx SoC Zynq XC7Z015/030.
2) 1Gbyte DDR3 memory for ARM CPU to run Linux
3) MicroSD for ARM CPU booting.
4) 2 channels of 12-bit ADC.
5) Programmable clock synthesizer and external 1PPS input.
6) GEN2 PCIe on top and bottom PCIe/104 connectors.
7) SATA Interface to PCIe/104 bottom connector or SEIC.
8) FMC LPC connector with I/O and single high-speed serial.
9) Single +5 or +12V power input (selectable).
10) 100-way SEIC peripheral interface connector.

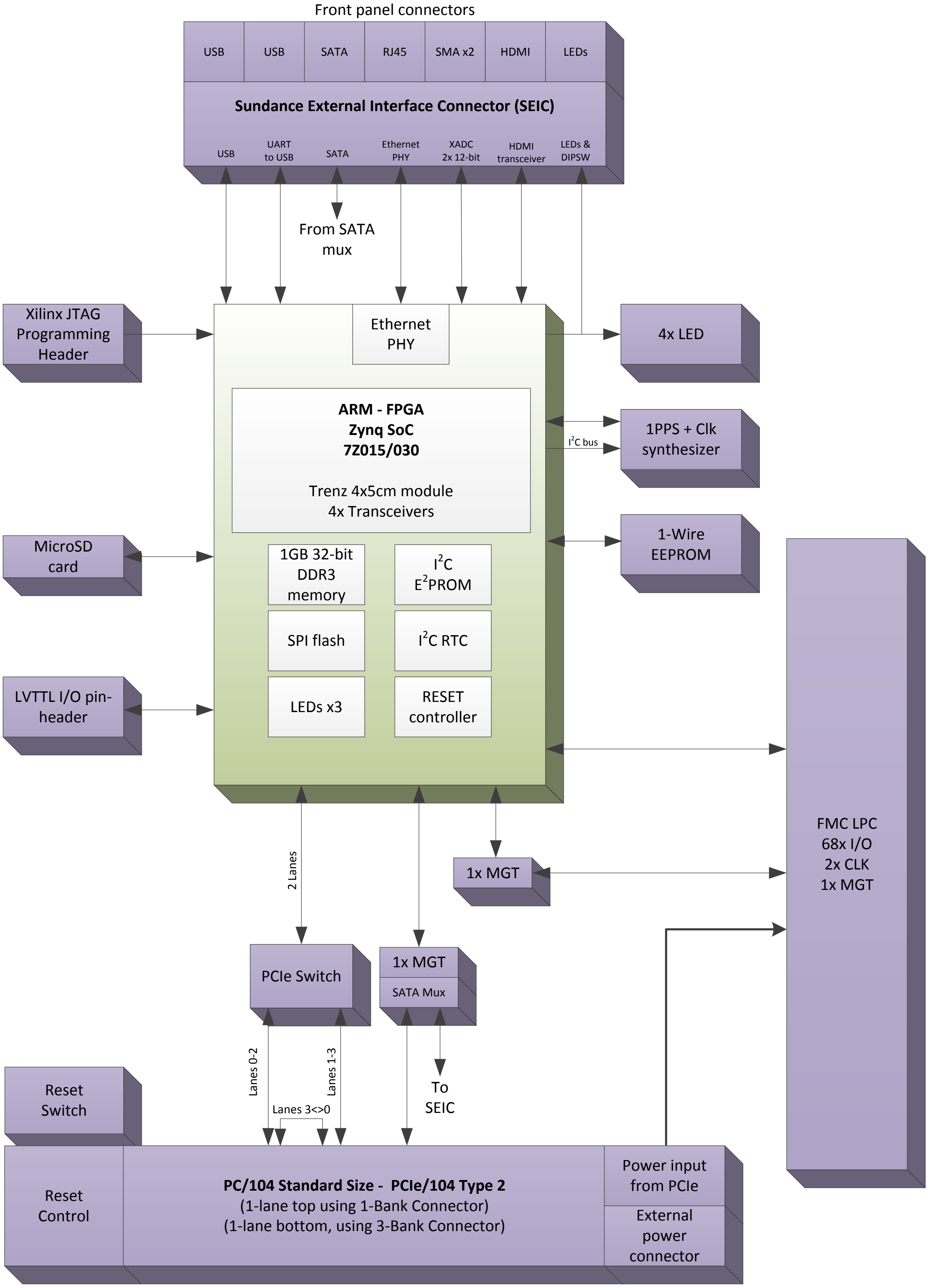
2 Notes

Several part numbers are described in the text, as HyperLink. These are possible part numbers, and alternative devices may be designed in at a later date.

2.1 Abbreviations / Definitions

ADC	Analog to Digital Converter.
DDR & DDR3	Dual Data Rate. An interface mechanism where data is transferred on both rising and falling clock edges. DDR3 memory is lower power and higher performance than its predecessor, DDR2.
DRAM	Dynamic RAM.
DVI	Digital Visual Interface. When used on its own in this document it refers to the digital portion of the connector's signals.
DVI-D	Digital video data only.
DVI-I	Digital and analog (VGA) data.
EEPROM	Also called E^2PROM (or just E^2). Electrically erasable and programmable ROM.
FPGA	Field Programmable Gate Array.
GMII	Gigabit Media Independent Interface.
GPIO	General Purpose Input Output.
I^2C	Inter-integrated Circuit. A two wire low speed serial interface.
MAC	Media Access Control.
Magnetics	Commonly used to refer to the inductors and transformers within the Ethernet signalling to the RJ45 connector.
MCB	Memory Control Block. A Spartan 6 internal hard core.
MicroSD	Small from factor variant of SD.
PHY	Commonly used to refer to the device that interfaces to the physical layer.
PPS	Pulse Per Second. A high accuracy external clock input.
RAM	Random Access Memory.
RGMII	Reduced pin count GMII.
RJ45	Commonly used to refer to the 8-pin connector used in Ethernet communication.
SATA	Serial Advanced Technology Attachment. Refers to the high-speed serial signalling on hard disk drives.
SD	Secure Digital. Related to the format of some non-volatile memory cards.
SEIC	Sundance External Interface Connector.
SLB	Sundance Local Bus. Multiple 8-bit LVDS synchronous busses.
SoC	System on a Chip.
SPB	Sundance Platform Bus. 50-way connector with multiple LVDS signals.
SSB	Sundance SRIO Bus.
USB	Universal Serial Bus.
VGA	Video Graphics Array. Used here to refer to the analog portion of the video signal.

3 Block Diagram



4 Circuit Description

The main component of the EMC²-DP is the Trenz TE0715 Zync based module. This module includes the Zync SoC, configuration device, Ethernet PHY and all power supply components necessary – with just a single 3.3V supply being required.

Another feature of the EMC²-DP is the use of an expansion board to the PCIe/104 form-factor. This expansion board, SEIC module, contains most of the I/O connectors and in some cases, interface circuitry too. The SEIC module is connected to the main board using a high density connector similar to that used for the Trenz FPGA module. When both boards are connected they lie in the same plane. See the PCB layout drawing for more details.

4.1 TE0715 Trenz FPGA Module – Technical Details Link

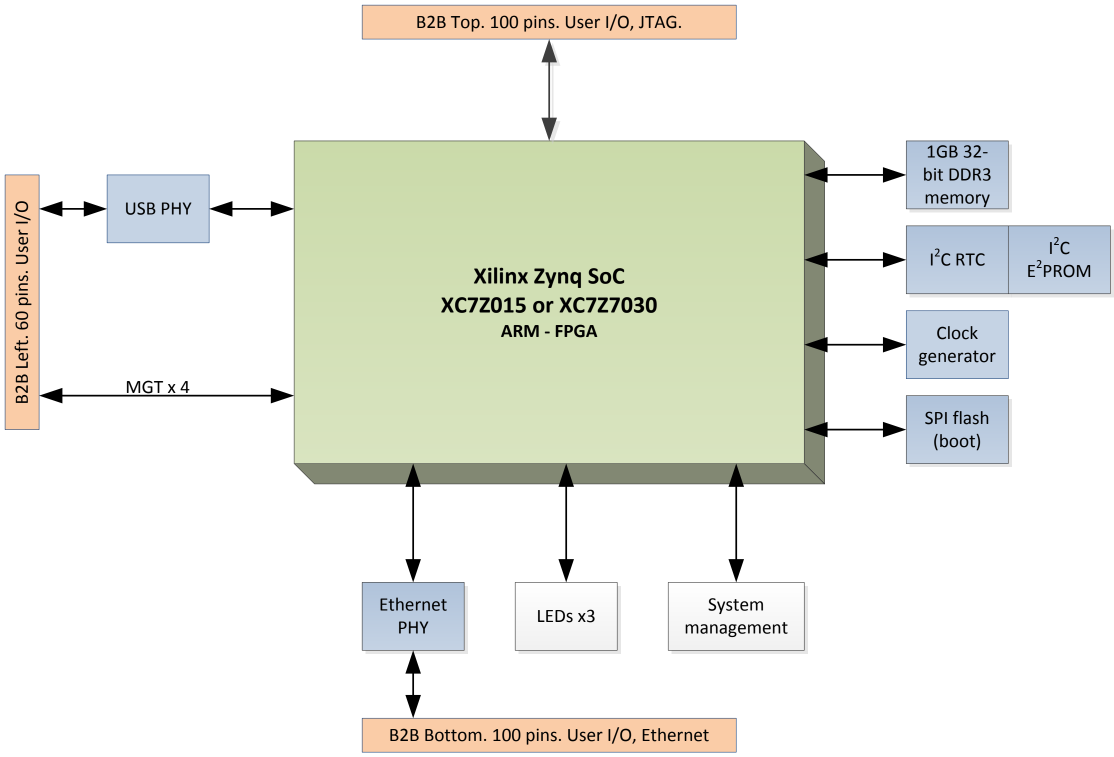


Figure 1 Block Diagram of Trenz 4x5 SoC Module

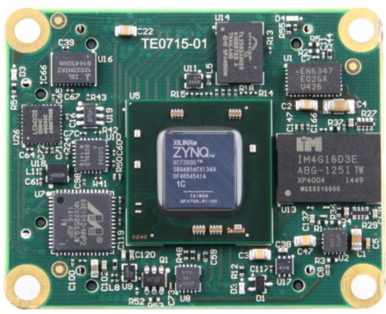


Figure 2 Top of Trenz 4x5 SoM Module - 1:1 Format

4.1.1 FPGA

The Xilinx XC7Z015 SoC incorporates a dual ARM A9 core running at up to 1GHz. The A9 based APU (Application Processor Unit) includes a 32kB level 1 cache and a 512kB level 2 cache. The level 1 caches are core independent but the level 2 cache is shared.

On-chip memory includes 256kB of RAM. This is supplemented by external memory interfaces which include DDR3, NOR and NAND flash.

Other peripherals include tri-speed Ethernet MAC, USB 2.0 OTG, CAN bus, SD controller, SPI, I^2C, UARTs and GPIO pins.

Coupled to this PS (Processing System) is the PL (Programmable Logic). This is typical Xilinx FPGA architecture and includes block RAMs, DSP blocks, LUTs, flip-flops and adders. A total of 74k logic cells and 380kB of RAM are provided.

Programmable I/O blocks support many signalling schemes from 1.2 to 3.3V. Four high speed (6.25Gb/s) serial links are provided which can be used as a PCIe interface.

For full details about the Zynq SoC FPGA Family; See the Xilinx website

For full details regarding the Trenz TE0715 module; see Trenz website and a User Manual, are available here for the TE0720:

4.1.2 Local Power Supplies

A range of Enpirion DC-DC step-down converters are used to create the local voltages of 1.8V, 1.5V and 1.0V. These can supply 1.5A, 1.5A and 4A respectively.

4.1.3 Configuration and Booting

The SoC'c configuration is volatile. When power is removed and then restored, the configuration is lost. Configuration of the device is typically performed using bitstreams stored in the SPI Flash device. The Trenz Wiki has detailed explanation of the boot process:

The basic procedure is as follows. The primary boot source is from the SoC SPI flash memory. Upon power-on, the Zynq will fetch the FSBL (first stage bootloader) from this device. This FSBL code initialises the peripherals and DDR3 memory, then proceeds to load object code for the PS and/or FPGA configuration data. Factory programmed FSBL does not have to configure the FPGA fabric.

The FSBL image cannot reside on the NAND flash; only on the SPI flash or external SD card.

The SSBL (second stage bootloader) is also usually stored in SPI flash. By default this loads a customised u-boot which is then responsible for loading the O/S. U-boot functionality is not essential and a user application could be directly loaded as an SSBL image.

The boot mode can be selected to be either JTAG (no boot), SPI flash, or external SD card.

The FPGA fabric can be loaded using u-boot or Linux (or JTAG).

4.1.4 JTAG

A 14-pin 2mm pitch pin header is provided for connection to a Xilinx USB Programmer (using the standard ribbon cable). This allows access to the internals of the SoC for configuration and debugging.

4.1.5 SoC Memory DDR3

Two 16-bit wide DDR3 memory devices are used on the Trenz module to provide **1GByte of** storage. This memory is directly accessible by the dual ARM9 processor cores.

4.1.6 SPI Flash

This serially accessible device holds the configuration for the SoC. It is 32Mbytes in capacity and implemented using a Winbond W25Q256FV device. See:

The SPI flash can be programmed using Vivado 2013.4 (or later) but NOT via the Impact programming tool.

The SPI flash can also be re-programmed by the Zynq from files stored on the SD card. U-boot commands *fatload* and *sf* are used for this.

The SPI resides on the Zynq MIO bus bits 1..6.

4.1.7 SD Card

A microSD (transflash) socket can accept a memory card. This socket is part of the mainboard and not the TE0715 module.

The TE0715 can boot directly from the SD card (bypassing the SPI flash).

The SD interface resides on the Zynq MIO bits 40..45.

4.1.8 I2C EEPROM

For smaller amounts of data, a separate non-volatile memory is provided which resides on an I^2C bus made available from the SoC.

This device can be used to store operating parameters separate from the configuration Flash. E.g. MAC address.

This I^2C interface resides on the Zynq MIO bits 48..49.

4.1.9 RTC

Real time clock functionality is provided by an Intersil ISL12020M RTC. This is backed-up with a 0.2F Super Cap in the event of power loss. This back-up lasts about 7 days and is located on the main board.

This I^2C interface resides on the Zynq MIO bits 48..49.

4.1.10 LEDs

Three user LEDs are provided directly on the SoC module. These are in addition to any that are available on the EMC^2-DP main circuit board.

4.1.11 Interface Connectors

The SoC is attached to the main board using high density Samtec connectors:

The pinout of these connectors is provided here.

4.1.12 Ethernet PHY

A single Ethernet PHY on the SoC (Marvell 88E1512) provides network connection on the SEIC via an RJ45 connector. This is a tri-mode device.

This interface resides on the Zynq MIO bits 16..27, 52, 53..

4.1.13 USB

A Microchip USB3320C provides a full featured hi-speed USB interface. This interface is made available on the SEIC and thus through the rear enclosure panel.

This interface resides on the Zynq MIO bits 28..39.

4.1.14 MIO Allocation

MIO Pin	Peripheral	Signal
MIO 0		
MIO 1	Quad SPI Flash	qspi0_ss_b
MIO 2	Quad SPI Flash	qspi0_io[0]
MIO 3	Quad SPI Flash	qspi0_io[1]
MIO 4	Quad SPI Flash	qspi0_io[2]
MIO 5	Quad SPI Flash	qspi0_io[3]
MIO 6	Quad SPI Flash	qspi0_sclk
MIO 7		
MIO 8		
MIO 9		
MIO 10	I2C 0	scl
MIO 11	I2C 0	sda
MIO 12	LED	LED3
MIO 13	LED	LED4
MIO 14	UART 0	rx
MIO 15	UART 0	tx
MIO 16	Enet 0	tx_clk
MIO 17	Enet 0	txd[0]
MIO 18	Enet 0	txd[1]
MIO 19	Enet 0	txd[2]
MIO 20	Enet 0	txd[3]
MIO 21	Enet 0	tx_ctl
MIO 22	Enet 0	rx_clk
MIO 23	Enet 0	rxd[0]
MIO 24	Enet 0	rxd[1]
MIO 25	Enet 0	rxd[2]
MIO 26	Enet 0	rxd[3]

MIO 27	Enet 0	rx_ctl
MIO 28	USB 0	data[4]
MIO 29	USB 0	dir
MIO 30	USB 0	stp
MIO 31	USB 0	nxt
MIO 32	USB 0	data[0]
MIO 33	USB 0	data[1]
MIO 34	USB 0	data[2]
MIO 35	USB 0	data[3]
MIO 36	USB 0	clk
MIO 37	USB 0	data[5]
MIO 38	USB 0	data[6]
MIO 39	USB 0	data[7]
MIO 40	SD 0	clk
MIO 41	SD 0	cmd
MIO 42	SD 0	data[0]
MIO 43	SD 0	data[1]
MIO 44	SD 0	data[2]
MIO 45	SD 0	data[3]
MIO 46		
MIO 47		
MIO 48	I2C 1	scl
MIO 49	I2C 1	sda
MIO 50		
MIO 51		
MIO 52		
MIO 53		

4.2 VITA57.1 FMC I/O Module

This LPC (low-pin count) variant provides 34 I/O and 2 clocks as differential pairs. I^2C and JTAG signals are also present. A provisional pin-out is provided at the end of this document.

4.3 Clock Synthesiser

This is a programmable device, via a serial interface from the SoC, that can generate a range of clocks. Several outputs are available and are connected to the clock capable pins of the SoC.

An SMA connector allows for an external clock input (shown as a 1PPS clock). Signal conditioning and filtering is provided as standard. This may be removed during build time to increase the frequency range. The external 1PPS clock must be an LVTTL signal of 1.8V.

This I^2C interface resides on the Zynq MIO bits 48..49.

4.4 SATA

The SoC provides 4 high speed serial interfaces, MGTs. One of these is connected to a MAX4986 via the SEIC to a SATA multiplexer/switch. E.g:

The outputs from this switch go to a standard SATA connector on the SEIC (accessible through the enclosure rear panel) and the other to the PCIe connector. The PCIe connection allows a SATA HD to be attached without cabling to a PCIe/104 Harddisk Module. Appropriate, like Sundance's FC003-D IP must be included within the Zynq fabric to allow the use of a SATA HDD.

4.5 USB

A Microchip USB3320C USB PHY is mounted directly on the SoC and drives the SEIC based USB connector (type A, USB host).

4.6 Ethernet

A single Ethernet PHY (Marvell 88E1512) provides network connection on the SEIC via an RJ45 connector. This is accessible through the enclosure rear panel.

It is a tri-mode (10/100/1000) device.

4.7 HDMI

Mounted on the SEIC module is an HDMI connector. An Analog Devices ADV7511KSTZ-P transmitter is employed to interface to the Zynq FPGA fabric. The interface to the ADV part includes:

- 24 data lines.
- Separate VSYNC and HSYNC.
- Single-ended clock input.
- Interrupt pin to Zync.
- I2C Bus.
- SPDIF out.

Fabric IP is used to drive the HDMI signals.

4.8 ADC

The Zync SoC includes dual ADCs. Refer to chapter 30 – *XADC Interface* of the Zynq TRM:

They are 12-bit 1MSPS converters and are driven from an analog multiplexer (internal the the Zynq). On the EMC^2-DP these inputs are driven from two SMA connectors on the SEIC module.

The XADC system can also measure on-chip temperature and power supplies.

4.9 UART

A 2-wire (Rx and Tx) UART interface can be provided by the SoC. These two wires are converted to a USB interface using a Silicon Labs CP2103GM (or similar) device. This is then made available on the SEIC module. A standard USB mini/micro to USB A cable can connect this to a host PC. OS drivers are readily available for this device.

This interface resides on the Zynq MIO bits 14-RX and 15-TX.

4.10 MEMS

A 3-axis accelerometer and magnetometer is present on the main board provided by InvenSense. The MPU-9150 device resides on a second I^2C bus.

This bus uses the Zynq MIO bits 10-SCL and 11-SDA.

4.11 LEDs

Four LED signals are driven directly from the SoC via current limiting resistors. They are made available to drive LEDs on the main PCIe/104 card and also on the SEIC module.

The LEDs connected to the PL should be driven with an open-collector type output pin from the Zynq. Those connected to the MIO should be driven using 3.3V LVTTL.

4.12 TTL I/O

An 8 pin 0.1" dual-in-line connector allows direct access to 4 SoC I/O pins. These have ESD (overvoltage and undervoltage) protection.

These pins support signal levels up to 1.8V only.

4.13 Reset

The Zync can be reset either from a push button or from the PCIe/104 connector.

When operating in standalone mode, a power-on reset circuit replaces the PCIe/104 reset.

The SoC employs a CPLD device to control power sequencing, reset generation, and initial Zynq configuration. The CPLD is a Lattice XO2-1200 and its design can be customised. The SC is part of the SoC JTAG chain. See the following link for operational details on this SC (System Controller):

Note that the functionality of the system reset pin to the SoC should be set to generate an interrupt and not a Zynq POR if a flash based OS is being used. This enables a proper OS shutdown to be performed.

4.14 1-Wire EEPROM

A Dallas/Maxim 1-Wire interface EEPROM connects to the PL part of the Zynq. This is operated at 3.3V and hence requires a bi-directional voltage convertor (MAX3394) to connect to the 1.8V Zynq I/O.

4.15 Power Supplies

Power is supplied to the board using the PCIe connector. Either the +5 or +12V supplies can be used; onboard voltage converters produce the necessary local voltages (listed below).

4.15.1 Power Rails

All local power rails are efficiently derived from either +5 or +12V.

Rail	How	Use	Current mA (typ.)	Current Measured
5.0	DCDC	Fan	100	100

4.16 Zync SoC

This device has the following interface connectivity:

Interface	Description	Comment(s)	Main, SoC or SEIC
DDR3	Memory for ARM.	DDR3 bank 0.	SoC
Flash	Used for device configuration.		SoC
SDcard	MicroSD.	Direct connection to Zynq.	Main
I2C EEPROM		Direct connection to Zynq.	SoC
USB	Host interface.	Available on the SEIC via type A connector.	SoC & Main
SATA	SATA interface.	PCIe/104 DOWN connector and SEIC.	SEIC
PCIe	1-lane PCIe.	PCI express UP connector.	Main
PCIe	1-lane PCIe.	PCI express DOWN connector.	Main
JTAG	For ARM and FPGA.	Header for FPGA configuration and ARM.	Main
MGT	1-lanes of high-speed serial.	FMC connector.	Main
LED	4 LEDs.		Main & SEIC
Clock Synth	Programmable PLL.	Used for the ADC sample clock. External clock input for 1PPS use.	Main
TTL	LVTTL (3.3V) I/O.	General purpose I/O to header.	Main
FMC		LPC signals.	Main
Ethernet PHY		Available when using an FMC or SEIC.	SoC
XADC	Two channel 12-bit ADC.	Analog connectors on SEIC.	SoC & Main

HDMI		Available when using an SEIC with the ADV7511.	SEIC
I2C	Serial bus.	Used to interface to the clock generator, RTC, I2C Eprom, etc.	SoC
RTC	Real Time Clock		SoC
Switch	For general purpose use.	8-bit DIP SW.	Main & SEIC
UART	Uses a USB to RS232 convertor.	Available when using an SEIC with SI CP2103GM.	SEIC
SPI Flash	Serial flash.		SoC

4.17 PCIe

The EMC2-DP board can operate in both host and add-on board modes.

The PCIe/104 connectors provide power (+12V, +5V, +3V3), global Reset, and PCI express connections to the host from the FPGA. An external connector is used to provide +12V power as the 1-bank connector does not supply this voltage.

The FPGA site provides 2 MGT lanes which are routed as PCIe to two ports of a 6-lane, 6-port PCIe packet switch (PEX8606 from PLX). The other 4 ports are routed to a signal switch (PI3PCIE3442 from Pericom).

The following diagram shows the lane connectivity when in host mode:

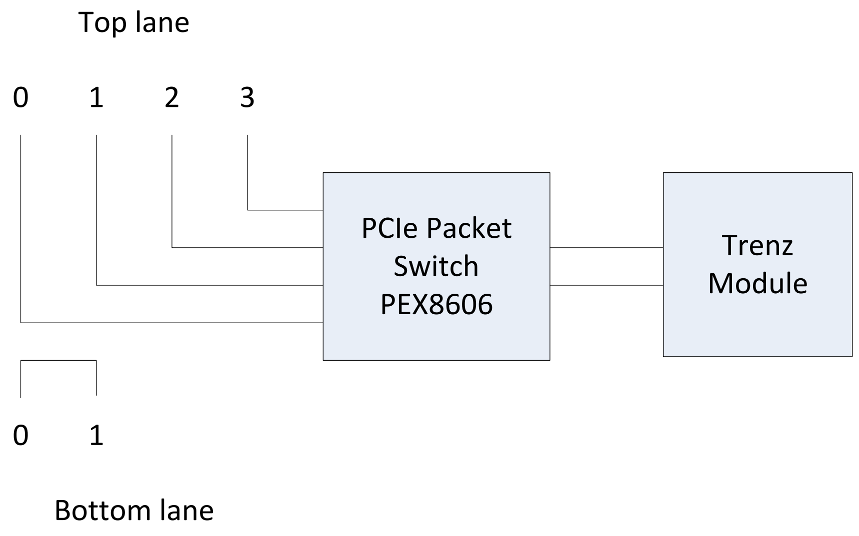


Figure 3 PCI Express Lanes in Host Mode

The effective loopback of bottom lanes 0 and 1 is a by-product of the signal switch operation. As the EMC2-DP is intended to form the base of the stack, this will have no consequence.

The following diagram shows the lane connectivity when in add-on mode:

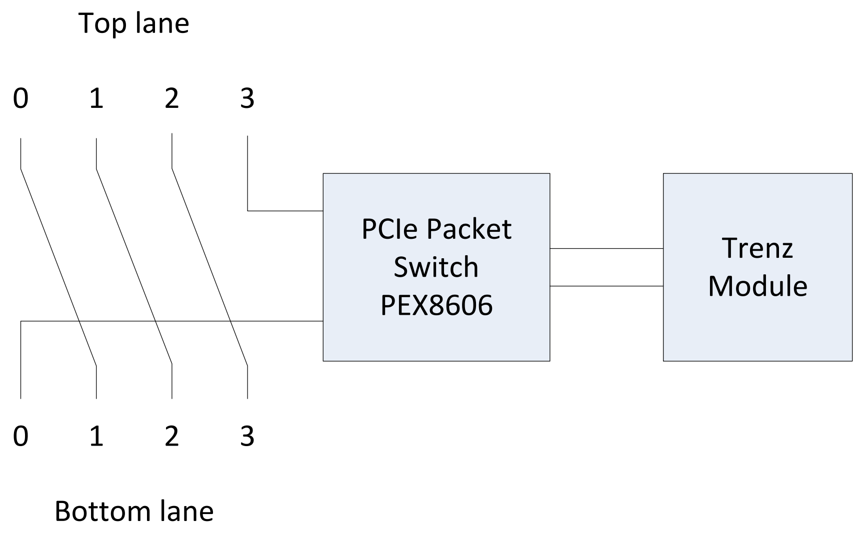


Figure 4 PCI Express Lanes in 'Add-On' Mode

As can be seen, the EMC2-DP can be used in either a stack-down or stack-up configuration.

The following diagram shows the lane connectivity as part of a stack:

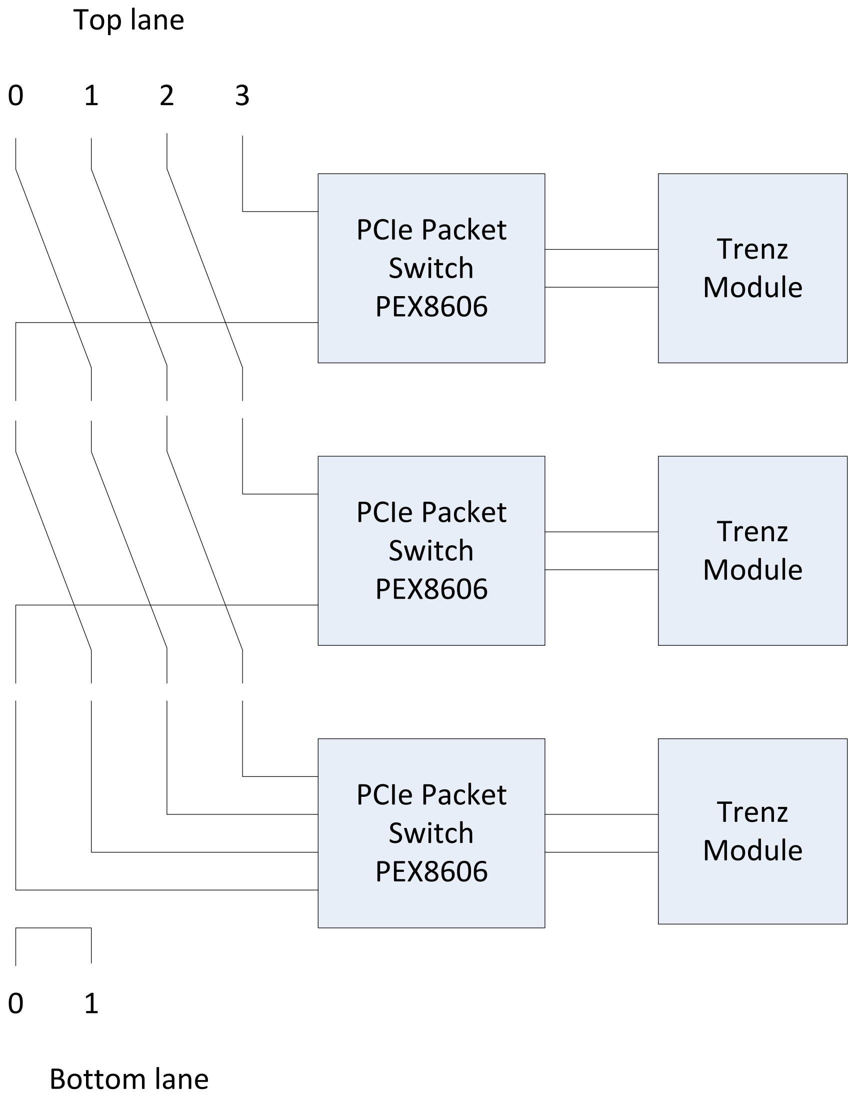
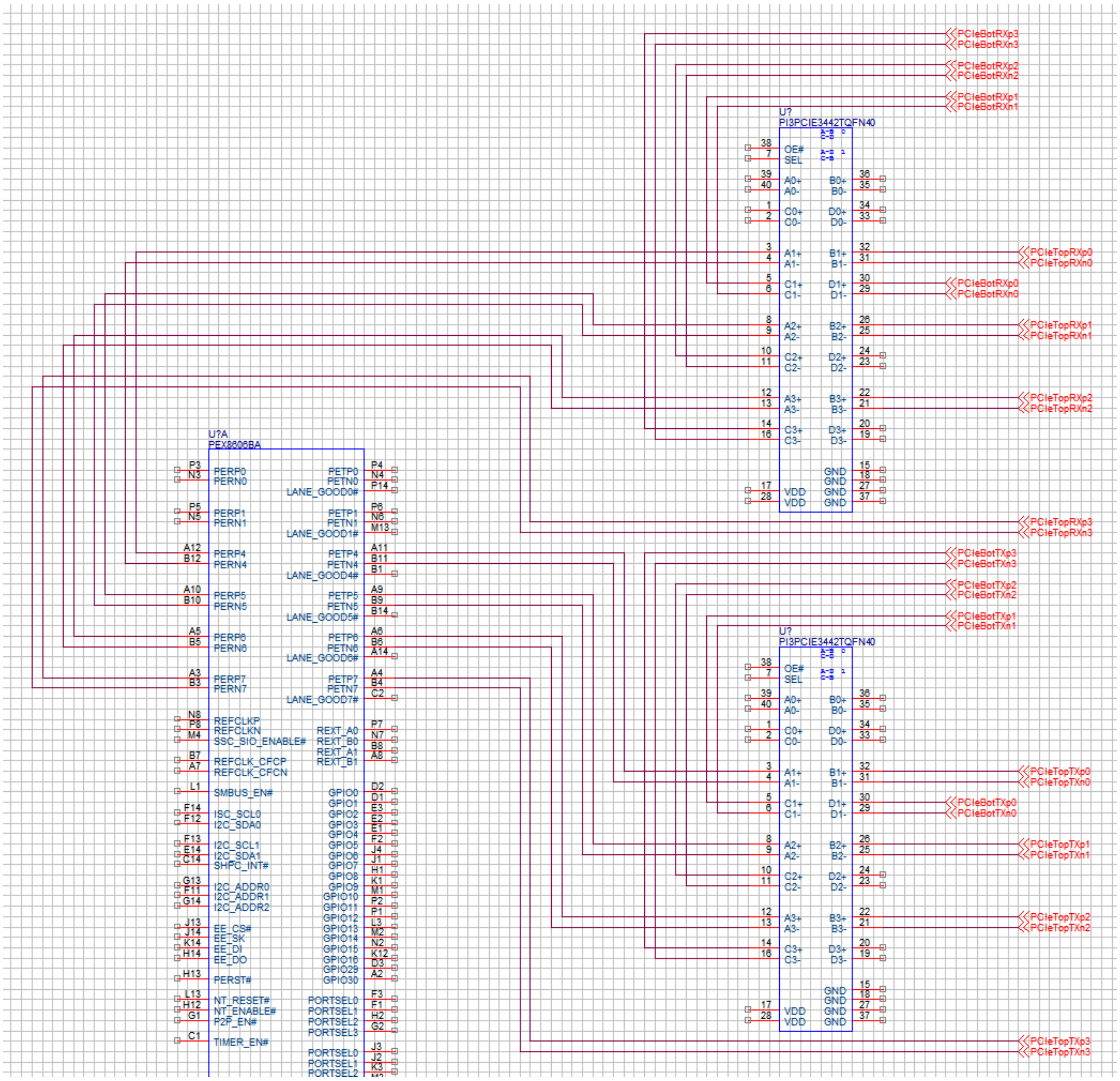


Figure 5 Multiple EMC²-DP in a PC/104 Stack

Two signal switches are required to route the PCIe lanes to the correct places. One switch for each of the Rx and Tx pairs.



The generation and routing of the PCIe reference clock is simpler. In host mode, a local oscillator is buffered and separate buffer outputs drive the four lanes to the top connector, the PCIe packet switch, and the Trenz module. The reference clocks to lanes 1-3 of the bottom connector are hardwired to the top lanes in the standard lane shift method. So, in host mode, 7 lanes are driven (not bottom lane 0 – which is unused in host mode).

In add-on mode, the buffer is disabled and hence the reference clock is sourced from either top lane 3 or bottom lane 0 via a selector that is switched using the CPU_DIR signal.

5 PCB Layout

The EMC²-DP is a PCIe/104 OneBank™ Form-Factor module without the "wing" extensions. The pictures below show the EMC²-DP in relation to an FMC front panel.

TO BE UPDATED

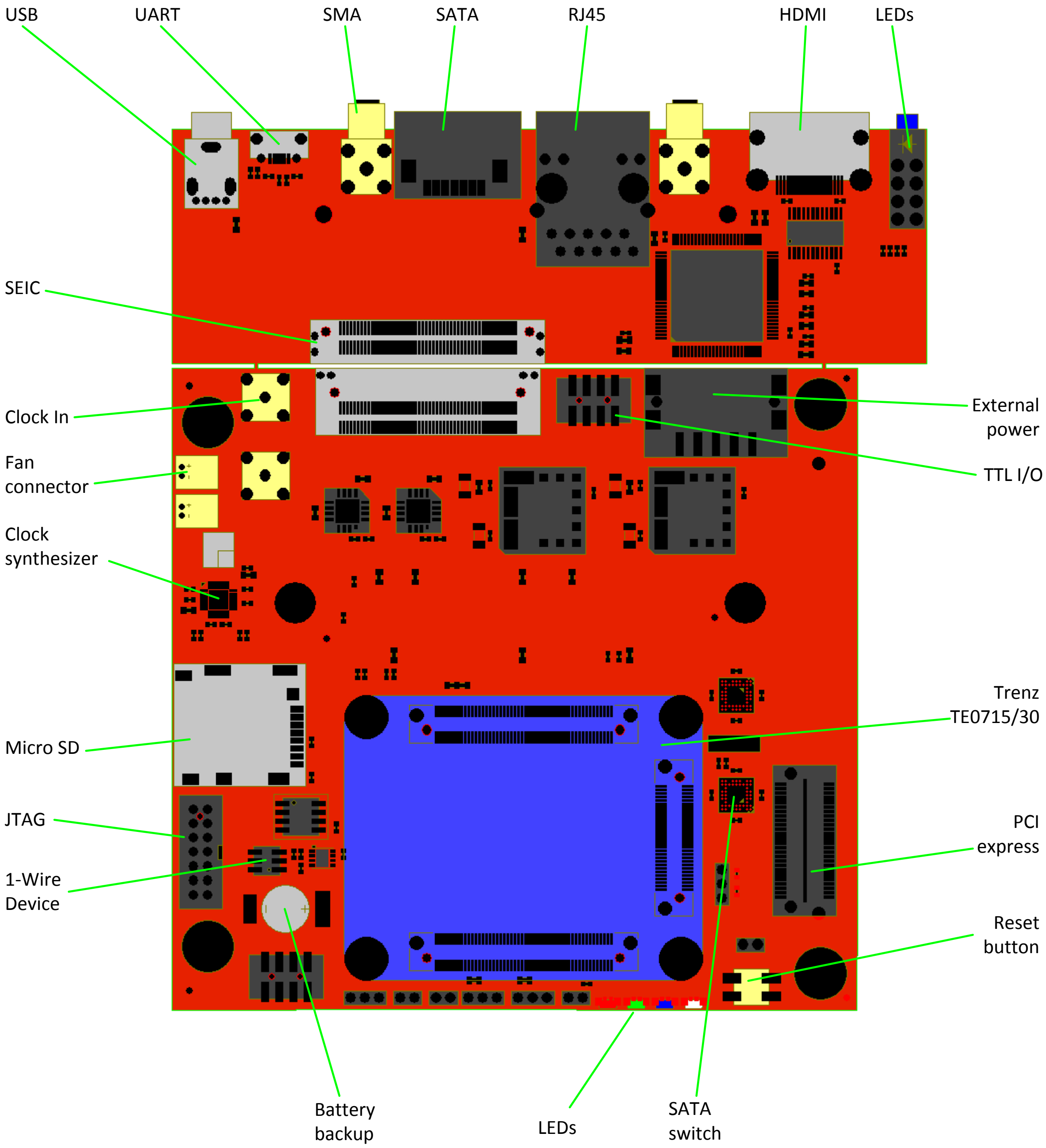


Figure 6 Top View of EMC²-DP

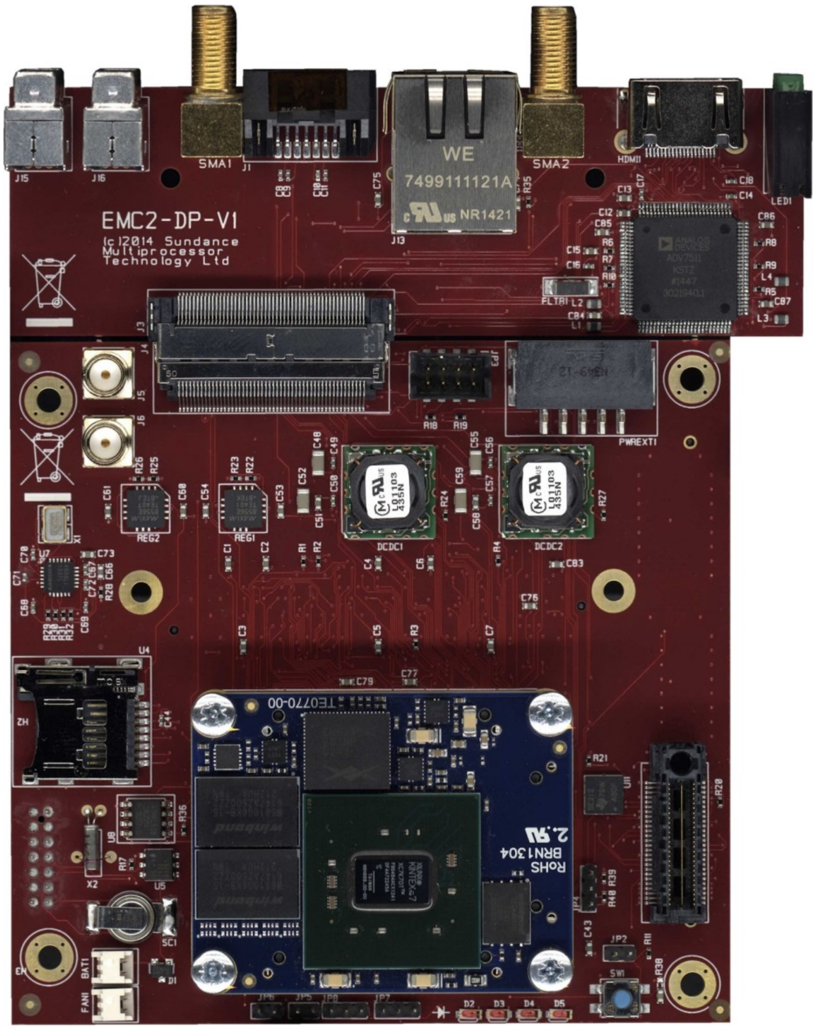


Figure 7 Top Photo of EMC²-DP - 1:1 Format

Bottom view

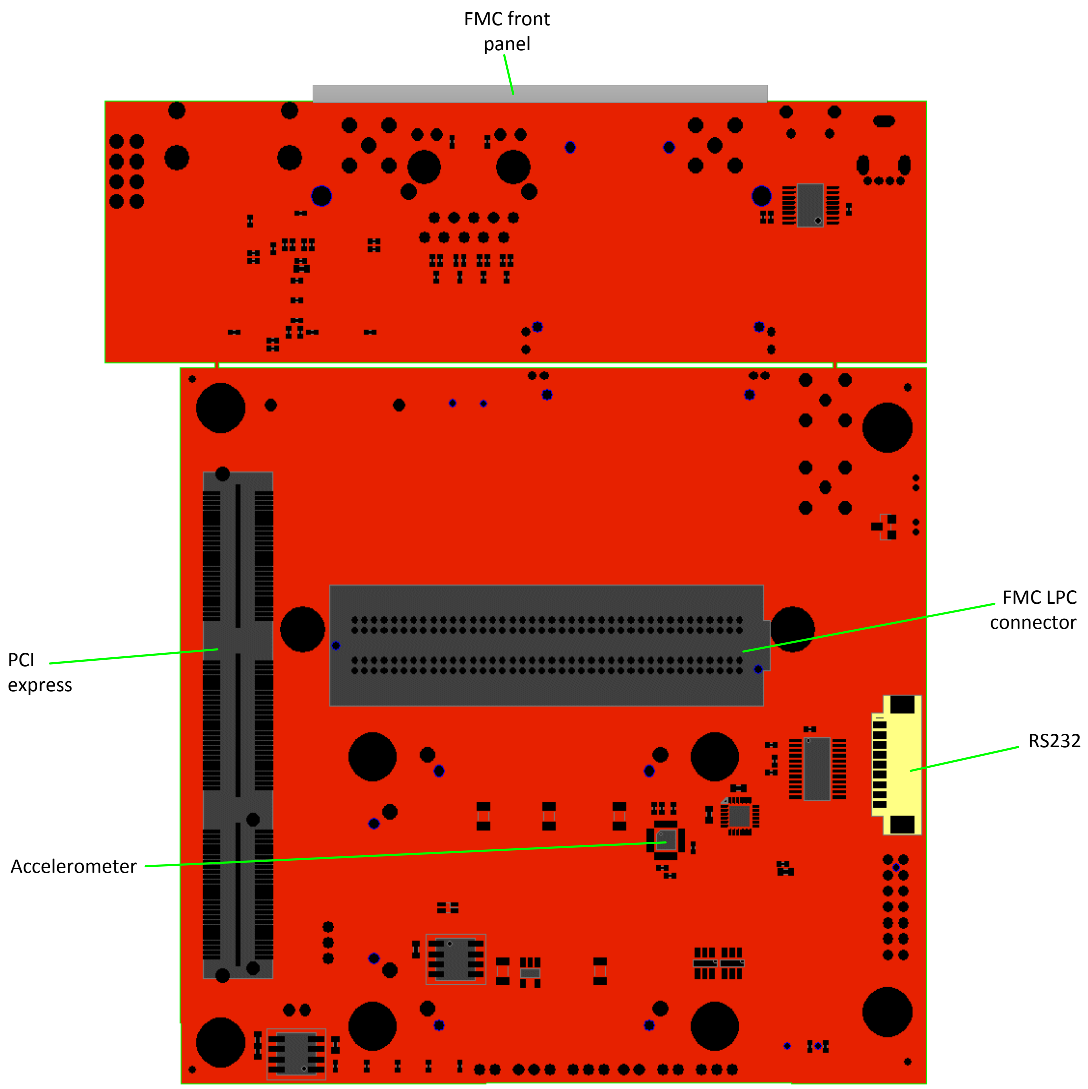


Figure 8 Bottom View of EMC²-DP

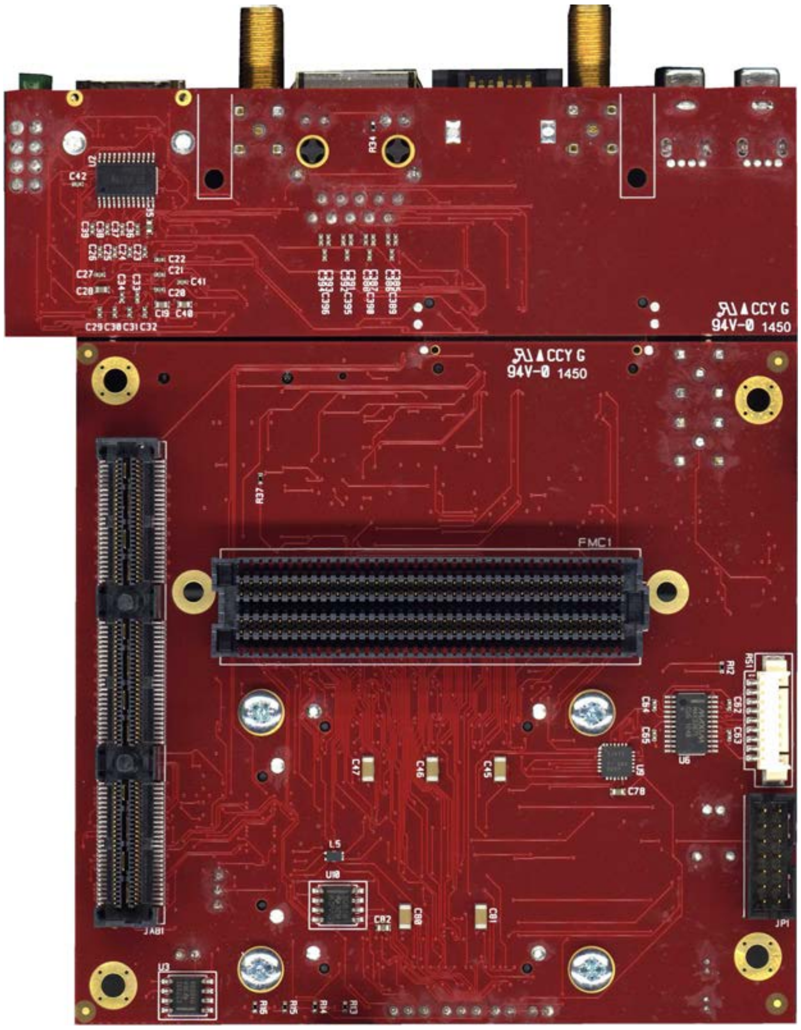


Figure 9 Bottom Photo of EMC²-DP - 1:1 Format

6 Physical Properties

Dimension, PC/104	90mm	96mm
Dimension, SEIC	33mm	106mm

Weight	

Voltage	Power (estimate)

RH	10-80%
Temperature	-10 to +40ºC -25 to +80ºC

MTBF	> 50,000 hours

7 FMC Pin-Out (provisional)

TO BE UPDATED

FMC pin	Signal	FPGA pin	FMC pin	Signal	FPGA pin
C10	FMC_LA6_P		D8	FMC_LA1_P	
C11	FMC_LA6_N		D9	FMC_LA1_N	
C14	FMC_LA10_P		D11	FMC_LA5_P	
C15	FMC_LA10_N		D12	FMC_LA5_N	
C18	FMC_LA14_P		D14	FMC_LA9_P	
C19	FMC_LA14_N		D15	FMC_LA9_N	
C22	FMC_LA18_P		D17	FMC_LA13_P	
C23	FMC_LA18_N		D18	FMC_LA13_N	
C26	FMC_LA27_P		D20	FMC_LA17_P	
C27	FMC_LA27_N		D21	FMC_LA17_N	
C30	FMC_SCL		D23	FMC_LA23_P	
C31	FMC_SDA		D24	FMC_LS23_N	
			D26	FMC_LA26_P	
			D27	FMC_LA26_N	
			D29	FMC_TDI	
			D30	FMC_TDO	
			D31	FMC_TMS	
			D33	FMC_TCK	

G2	FMC_CLK1_P		H1	FMC_VREF	
G3	FMC_CLK1_N		H2	FMC_PRSNT	
G6	FMC_LA0_P		H4	FMC_CLK0_P	
G7	FMC_LA0_N		H5	FMC_CLK0_N	
G9	FMC_LA3_P		H7	FMC_LA2_P	
G10	FMC_LA3_N		H8	FMC_LS2_N	
G12	FMC_LA8_P		H13	FMC_LA7_P	
G13	FMC_LA8_N		H14	FMC_LA7_N	
G15	FMC_LA12_P		H16	FMC_LA11_P	
G16	FMC_LA12_N		H17	FMC_LA11_N	
G18	FMC_LA16_P		H19	FMC_LA15_P	
G19	FMC_LA16_N		H20	FMC_LA15_N	
G21	FMC_LA20_P		H22	FMC_LA19_P	
G22	FMC_LA20_N		H23	FMC_LA19_N	
G24	FMC_LA22_P		H25	FMC_LA21_P	
G25	FMC_LA22_N		H26	FMC_LA21_N	
G27	FMC_LA25_P		H28	FMC_LA24_P	
G28	FMC_LA25_N		H29	FMC_LA24_N	
G30	FMC_LA29_P		H31	FMC_LA28_P	
G31	FMC_LA29_N		H32	FMC_LA28_N	
G33	FMC_LA31_P		H34	FMC_LA30_P	
G34	FMC_LA31_N		H35	FMC_LA30_N	
G36	FMC_LA33_P		H37	FMC_LA32_P	
G37	FMC_LA33_N		H38	FMC_LA32_N	
G39	FMC_VADJ		H40	FMC_VADJ	

8 Trenz Module Pin-Out

To Be Added

9 Verification, Review & Validation Procedures

To be carried out in accordance with the Sundance Quality Procedures (ISO9001).

10 Safety

This module presents no hazard to the user when in normal use.

11 EMC

This module is designed to operate from within an enclosed host system, which is built to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate enclosure.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.

12 Ordering Information

Order number:

EMC²-DP-xx-y

xx:

15	Zync Z7015
30	Zync Z7030

y:

C =	Commercial temperature
I =	Industrial temperature