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Product Specification for SMT-FMC510L

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Revision History

Issue	Changes Made	Date	Initials
1	First draft.	3/1/2018	GKP
2	Correction to RS422 transceiver part number	16/1/2018	GKP
3	LSHM connector pin-out mirrored on main FMC board.	23/1/2018	GKP
4	Added PWRGD to FMC pin D21.	24/1/2018	GKP
5	Added decoder/encoder register settings.	8/3/2018	GKP
6	Added detail on RS422 transceiver FPGA interface voltages.	22/3/2018	GKP

Table of Contents

1 Introduction

The SMT-FMC510L is an FMC module with a low pin count connector (LPC) and is a support module for the Tulipp project.

It is primarily designed to attach to the EMC2-DP FMC PCIe104 carrier board and provide analog video and serial interfaces.

Connectivity is via BNC connectors on the main FMC PCB, BNC connectors on an adaptor PCB, and two 20-way latching DIL pin headers.

2 Related Documents

2.1 Referenced Documents

ADV7180 video decoder datasheet (http://www.analog.com/en/products/audio-video/video-decoders/adv7180.html)

ADV7390 video encoder datasheet (http://www.analog.com/en/products/audio-video/video-encoders/adv7390.html)

ADV7393 circuit note (http://www.analog.com/en/design-center/reference-designs/hardware-reference-design/circuits-from-the-lab/cn0101.html)

LMH0303 SDI cable driver datasheet (http://www.ti.com/lit/ds/symlink/lmh0303.pdf)

LMH0303 eval board user guide (http://www.ti.com/lit/ug/snlu054/snlu054.pdf)

LMH0344 SDI cable equalizer datasheet (http://www.ti.com/lit/ds/symlink/lmh0344.pdf)

LMH0344 eval board user guide (http://www.ti.com/lit/ug/snlu130/snlu130.pdf)

TLV320AIC3204 Audio CODEC datasheet (http://www.ti.com/lit/ds/symlink/tlv320aic3204.pdf)

SN65MLVD20xx LVDS line driver datasheet (http://www.ti.com/lit/ds/symlink/sn65mlvd204a.pdf)

Intersil ISL80102 LDO datasheet (https://www.intersil.com/en/products/power-management/linear-regulation/linear-regulators/ISL80102.html)

CPC1014N solid state relay datasheet (http://www.ixysic.com/home/pdfs.nsf/www/CPC1014N.pdf/$file/CPC1014N.pdf)

Trenz TE0715 documentation (https://wiki.trenz-electronic.de/display/PD/TE0715)

Sundance EMC² (http://www.sundance.technology/som-cariers/pc104-boards/emc%C2%B2-dp-carrier/)

2.2 Applicable Documents

ANSI/VITA 57.1-2008 FMC Specification

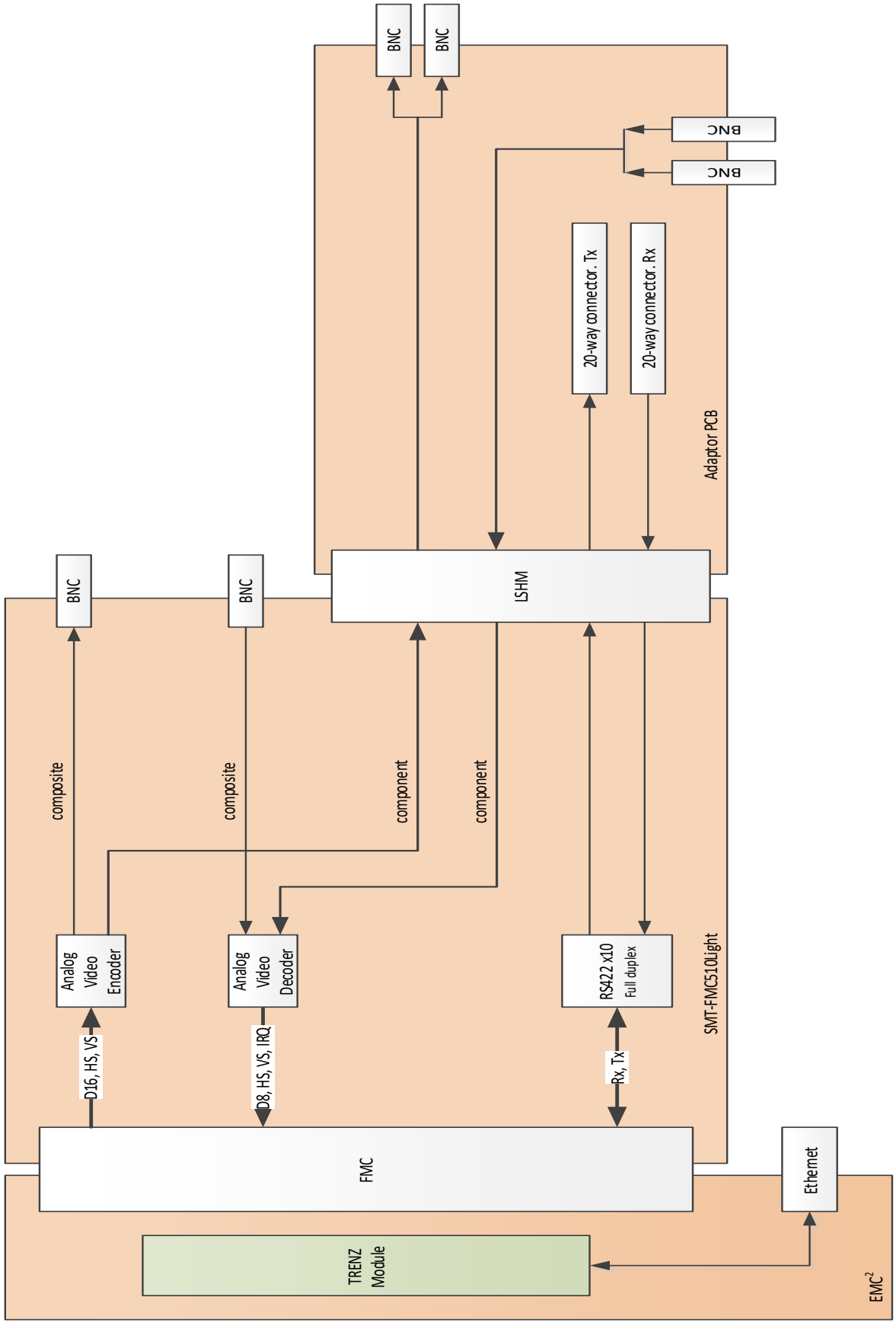
3 Acronyms, Abbreviations and Definitions

3.1 Acronyms and Abbreviations

ADC	Analog to Digital Converter.
BNC	Co-axial connector (Bayonet Neill-Concelman).
CVBS	Colour, Video, Blanking and Sync.
DAC	Digital to Analog Converter.
FMC	FPGA Mezzanine Card.
FPGA	Field Programmable Gate Array.
GPIO	General Purpose Input Output.
HPC	High Pin Count.
HSYNC	Horizontal SYNC.
I^2C	Inter-integrated Circuit. A two wire low speed serial interface.
LED	Light Emitting Diode.
LPC	Low Pin Count.
LSHM	Samtec high-speed hermaphroditic connector.
MGT	Multi-Gigabit Transceiver.
PCB	Printed Circuit Board.
Rx	Receive.
SDI	
SEIC	Sundance External Interface Connector.
SYNC	Synchronising.
Tx	Transmit.
UART	Universal Asynchronous Receiver Transmitter.
VSYNC	Vertical SYNC.

4 Functional Description

4.1 Block Diagram



4.2 Module Description

This module is based on the FMC specification with the addition of an additional adapter PCB. The adapter PCB is optional and only required if interfaces other than analog video are needed.

The following interfaces are provided on the main FMC module:

- BNC connector carrying analog video out.
- BNC connector carrying analog video in (optional).
- LSHM connector carrying:
    - One analog video output
    - One analog video input
    - 10 pairs of full-duplex RS422

The following are the interfaces presented to additional connectors when using the adapter PCB:

- BNC connector carrying analog video out.
- BNC connector carrying analog video in (optional).
- 2 x 20-way connectors with 10 full-duplex RS422 channels.

4.2.1 Mechanical Interface

The FMC module's front panel has two HD-BNC connectors (for analog video), and a high density Samtec connector (LSHM-150-01-L-RH-A-S-K-TR).

The adapter PCB has two HD-BNC connectors (for analog video output), and two standard 2x10 0.1" pitch latching pin-headers.

A cable may be used between the main and adapter PCBs if the adapter PCB needs to be located away from the FMC module.

4.3 Electrical Interface

4.3.1 FMC

This connector is the LPC variant.

This connector and interface provides 34 differential pairs or 68 single ended signals. The I/O voltage of the FPGA that drives these signals **should be set to 3.3V**. This is accomplished by a 2mm jumper system on the EMC² board.

A single multi-gigabit interface is composed of a transmit differential pair, a receive differential pair, and a differential clock. The clock is generated on the FMC module as 148.5MHz LVDS.

+12V (2 pins) and +3.3V (4 pins) power is available on this connector.

An I²C interface is defined in the FMC specification. This is primarily used to access a serial EEPROM used to store FMC module ID information.

A separate I²C bus is also included which connects the Trenz module's FPGA to the programmable devices on the SMT-FMC510L.

A power_good signal is generated on the module and fed back to the FMC carrier on pin D21. This is essentially a 10k pull-up to 1.8V.

An active low RESET is provided from the carrier to the module.

4.3.2 Video encoder

The video encoding is provided by an ADV7393BCPZ.

This device has a 16-bit parallel interface connected to the FPGA via the FMC connector. Other control signals consist of HSYNC, VSYNC and an I²C bus for control register access.

A single CVBS video output is available on the main FMC module. If component video output is needed, the extra two signals are available on the adapter board.

The encoder device physically consists of 3 DACs. The device datasheet page 49 lists all possible DAC output combinations. Essentially, for SD modes this includes CVBS on DAC1 (the BNC on the FMC module), Y/C from DACs2&3 (the BNCs on the adaptor board), YPbPr and RGB (both using all 3 BNCs).

For ED and HD modes, CVBS and Y/C are not supported, only RGB and YPbPr.

4.3.3 Video decoder

Video decoding is provided by an ADV7180BCPZ. This device is optional.

This device has an 8-bit parallel interface connected to the FPGA via the FMC connector. Other control signals consist of HSYNC, VSYNC, INTerrupt and an I²C bus for control register access.

A single CVBS video input is available on the main FMC module. If component video input (Y/C or Y/Pb/Pr) is needed, the extra signals are available on the adaptor board (specify this requirement when ordering).

The decoder device is physically a multiplexed single ADC with 3 analog inputs. The datasheet page 20 lists the available input combinations. Essentially, CVBS can be

input using the FMC module's BNC. Y/C and YPbPr need the BNCs on the FMC module and those on the adaptor board.

4.3.4 RS422

Each of the 10 RS422 interfaces are driven from a simple UART within the FPGA.

Ten MAX13433 full-duplex transceivers are used. The differential signals are connected to the LSHM connector of the FMC module. The adaptor board then presents these to two 20-pin 0.1" pitch latching pin headers (eg Omron XG4A-2031).

The transceiver's receiver interface is permanently enabled. The transmit interface is enabled from an FPGA signal (one per channel).

The RS422 Tx enable signals are driven directly from the Trenz module's FPGA.

All of the RS422 transceivers use the voltage Vadj (typically set on the FMC carrier) for the interfacing to the FPGA. When using the EMC^2 for example, Vadj is set using two jumper blocks. These should be positioned so as to reflect the capabilities of the FPGA being used. For a Xilinx Z7015 based module, any Vadj setting can be used as this device only has HR pins and can accept 3.3V signals. For the Xilinx Z7030 based module, some pins are NOT 3.3V tolerant so Vadj should be set to 1.8V.

4.3.5 LEDs

Two LEDs are directly driven from the FPGA via the FMC connector pins LA32_P and LA32_N. The FPGA's output needs to be set to logic '0' to illuminate the LED.

5 Quality Procedures

To be carried out in accordance with the Sundance Quality Procedures (BSI9001:2015).

See: http://quality.sundance.com/index.php/Main_Page

6 Validation Procedures

7 Circuit Description / Diagrams

8 Footprint

8.1 Top View

8.2 Bottom View

TBD

9 Pinout

9.1 LSHM (FMC module)

Signal	Pin	Pin	Signal
GND	2		
LED2	22		
LED1	24	17	GND
LED0	26		
GND	28	35	RX422N_9
RX422N_8	38	37	RX422P_9
RX422P_8	40	39	RX422N_7
RX422N_6	42	41	RX422P_7
RX422P_6	44	43	GND
RX422N_4	46	45	RX422N_5
RX422P_4	48	47	RX422P_5
RX422N_2	50	49	RX422N_3
RX422P_2	52	51	RX422P_3
RX422N_0	54	53	RX422N_1
RX422P_0	56	55	RX422P_1
GND	58	57	TX422N_9
TX422N_8	60	59	TX422P_9
TX422P_8	62	61	TX422N_7
TX422N_6	64	63	TX422P_7
TX422P_6	66	65	TX422N_5
TX422N_4	68	67	TX422P_5
TX422P_4	70	69	GND
TX422N_2	72	71	TX422N_3
TX422P_2	74	73	TX422P_3
TX422N_0	76		
TX422P_0	78		
TX422N_1	80		
TX422P_1	82		
GND	88	87	GND
Video In Pb	90	89	Video Out Chroma
Video In Pr	92	91	Video Out Luma
GND	94	93	GND
GND	98	97	GND
3.3V	100	99	3.3V

Notes: Not all pins shown.

The Samtec LSHM series of connectors are hermaphroditic. This means that two of the same connector can be inverted and connected together. The consequence of this is that the LSHM connector on the adapter board has a mirror-image pin-out of that on the main FMC module. That is, pin 1 will connect to pin 2, pin 3 to 4, etc.

The pin-out given here is that of the LSHM connector on the main FMC module, NOT that of the adapter board.

The RS422 channels comprise of a differential pair for receive, RX422P and RX422N, and a similar pair for transmit, TX422P and TX422N.

9.2 RS422 Pin Headers

Each of the following tables shows the pin-outs of the dual in line pin-headers. These are 20 way headers of 2 columns of 10 rows, with a 0.1” pin pitch.

Signal	Pin	Pin	Signal
RX422P_0	1	2	RX422N_0
RX422P_1	3	4	RX422N_1
RX422P_2	5	6	RX422N_2
RX422P_3	7	8	RX422N_3
RX422P_4	9	10	RX422N_4
RX422P_5	11	12	RX422N_5
RX422P_6	13	14	RX422N_6
RX422P_7	15	16	RX422N_7
RX422P_8	17	18	RX422N_8
RX422P_9	19	20	RX422N_9

Signal	Pin	Pin	Signal
TX422P_0	1	2	TX422N_0
TX422P_1	3	4	TX422N_1
TX422P_2	5	6	TX422N_2
TX422P_3	7	8	TX422N_3
TX422P_4	9	10	TX422N_4
TX422P_5	11	12	TX422N_5
TX422P_6	13	14	TX422N_6
TX422P_7	15	16	TX422N_7
TX422P_8	17	18	TX422N_8
TX422P_9	19	20	TX422N_9

9.3 FMC Pinout

C1	GND
C2	
C3	
C4	GND
C5	GND
C6	
C7	
C8	GND
C9	GND
C10	RX0
C11	TX0
C12	GND
C13	GND
C14	RX3
C15	TX3
C16	GND
C17	GND
C18	DVO14
C19	DVO15
C20	GND
C21	GND
C22	SCLK
C23	SDATA
C24	GND
C25	GND
C26	DVIN7
C27	DVIN6
C28	GND
C29	GND
C30	SCL
C31	SDA
C32	GND
C33	GND
C34	GA0
C35	12PV
C36	GND
C37	12PV
C38	GND
C39	3P3V
C40	GND

D1	PG
D2	GND
D3	GND
D4	GCKP
D5	GCKN
D6	GND
D7	GND
D8	DVO0
D9	DVO1
D10	GND
D11	DVO6
D12	DVO7
D13	GND
D14	RX2
D15	TX2
D16	GND
D17	RX6
D18	TX6
D19	GND
D20	DVCKO
D21	PWRGD
D22	GND
D23	TXEN2
D24	TXEN3
D25	GND
D26	
D27	DVINT
D28	GND
D29	
D30	
D31	
D32	3P3VA
D33	
D34	
D35	GA1
D36	3P3V
D37	GND
D38	3P3V
D39	GND
D40	3P3V

G1	GND
G2	DVCKI
G3	LED2
G4	GND
G5	GND
G6	DVO8
G7	DVO9
G8	GND
G9	DVO10
G10	DVO11
G11	GND
G12	DVO12
G13	DVO13
G14	GND
G15	RX5
G16	TX5
G17	GND
G18	RX8
G19	TX8
G20	GND
G21	TXEN0
G22	CKSEL
G23	GND
G24	RST\
G25	TXEN1
G26	GND
G27	DVI5
G28	DVI4
G29	GND
G30	DVI1
G31	DVI0
G32	GND
G33	TXEN8
G34	TXEN9
G35	GND
G36	RX9
G37	TX9
G38	GND
G39	VADJ
G40	GND

H1	VREF
H2	PRSNT
H3	GND
H4	DCKP
H5	DCKN
H6	GND
H7	DVO2
H8	DVO3
H9	GND
H10	DVO4
H11	DVO5
H12	GND
H13	RX1
H14	TX1
H15	GND
H16	RX4
H17	TX4
H18	GND
H19	RX7
H20	TX7
H21	GND
H22	DVOVS
H23	DVOHS
H24	GND
H25	DVIVS
H26	DVIHS
H27	GND
H28	DVI3
H29	DVI2
H30	GND
H31	TXEN4
H32	TXEN5
H33	GND
H34	TXEN6
H35	TXEN7
H36	GND
H37	LED0
H38	LED1
H39	GND
H40	VADJ

DVO	Video Out bus to encoder.
DVI	Video In bus from decoder.
-VS	Vertical Sync.
-HS	Horizontal Sync.
RX	RS422 receive.
TX	RS422 transmit.
TXEN	RS422 Transmit Enable.
DCKP/N	Video Decoder Clock output (differential).
DVCKI	Video Encoder Clock input.
DVCKO	Video Decoder Clock output OR local 29.5MHz oscillator.
CKSEL	Selector for DVCKO.

10 Support Packages

10.1 Video reference design for Trenz Z7030

This reference design outputs captured images from analog video input, to analog video output.

It shows how to setup the two analog video devices, and how to stream video data to/from the Trenz module's FPGA.

10.2 Video output reference design

This reference design outputs a video test pattern as CVBS on DAC1, and Y/C on DACs2&3.

10.3 RS422 reference design

Each of these interfaces is implemented using a UART.

11 Encoder / Decoder Register Settings

The encoder and decoder devices contain many registers. Most of these can remain in their default condition.

No register changes are necessary in order to configure the video decoder for NTSC (SD) input (YCbCr output).

In order to configure the video encoder for NTSC output (SD) with YCbCr input, the following registers need to be altered:

Register (hex)	Value	Comment
17	02	Software reset.
00	1C	All DACs on.
00	10	DAC1 on, DACs 2&3 off.
01	00	No change.
80	10	No change.
82	CB	Active video edge control enabled. Pixel data valid enabled.

12 Physical Properties

Dimensions		
Weight		
Supply Voltages		
Supply Current	+12V	
	+5V	
	+3.3V	
	-5V	
	-12V	
MTBF		

13 Safety

This module presents no hazard to the user when in normal use.

14 EMC

This module is designed to operate from within an enclosed host system, which is built to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.

15 Ordering Information

SMT-FMC510L	Standard part with Video output, RS422, and adapter board.
SMT-FMC510L-VIN	As above but also with Video input. Please specify whether the video input BNC connectors are required on the adapter board.