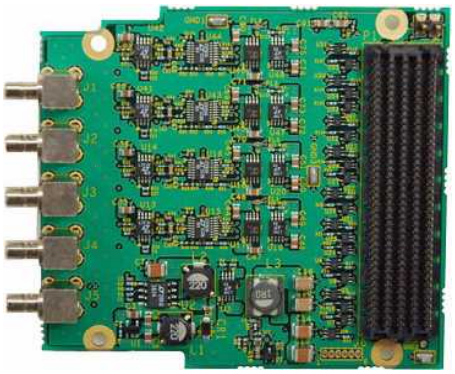
RFM-ADCFN04-D250KH
(FMC AD board)
Hardware Reference Manual
Ver.1.0



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Revision History

Version	Date	Change Made
ver1.0	2017/10/05	First Release

Table of Contents

1) Preface

Thank you for choosing **RFM-ADCFN04-D250KH** FMC board.
This manual describes the features and specifications of the **RFM-ADCFN04-DS250KH** FMC board.
Read and understand the contents of this manual before operating this board.

K.K.Rocky reserves the right to revise this document and to make changes without notice.

2) Safety Instructions

Always read the safety instructions carefully.

Cautions

- **If smoke or an abnormal odor is detected from the FMC board, power off and stop using the FMC board.**
  Continuous use of FMC board under these conditions might cause fire or permanent damage to the system. Contact K.K.Rocky to test and repair.

- **Do not attempt to disassemble and modify this board.**
  Disassembly and modification could cause fire or electric shock.
  Please contact K.K.Rocky for any repair and test service.

- **Never allow any liquids to spill on the FMC board, and never expose FMC board to water or moisture**.
  Exposure to liquid or moisture could cause electric shock or fire.

- **Avoid excessive vibration and any impact or shock to the FMC board.**
  Neglect could result in any damage on the board.

- **Avoid handling the FMC board while it is powered. Only handle by the edges to minimize the risk of electrostatic discharge damage.**

- **if the FMC board has been dropped and damaged, stop using the board and contact K.K.Rocky to repair.**

- **Never place the board where it will be exposed to excess heat, such as in direct sunlight, or near heater.**

1. Introduction

The RFM-ADCFN04-D250KH is an ANSI/VITA57-1 compliant FPGA Mezzanine Card (FMC) which offers multi-purpose 4-channel AD converter up to 250KSPS.
It works on a High Pin Count (HPC) site of FMC carrier board from K.K.Rocky or third party.

2. Main components

The main components of the board are listed on Table 2-1.

Table 2-1 Main Components

Item	Description	Remarks
FMC connector (HPC)	ASP-134488-01 (SAMTEC)	
AD converter	LTC2376CMS-16 (Linear Technology)	
ADC Driver	LT6350CMS (Linear Technology)	
Voltage Reference	ADR445ARMZ (Analog Devices)	5V
EEPROM (I2C)	BR24L01AFV-WE2 (Rohm)	
Front side Coaxial connector	414026-3 (Tyco)	

3. Block Diagram

Figure 3-1 shows the block diagram of the board.

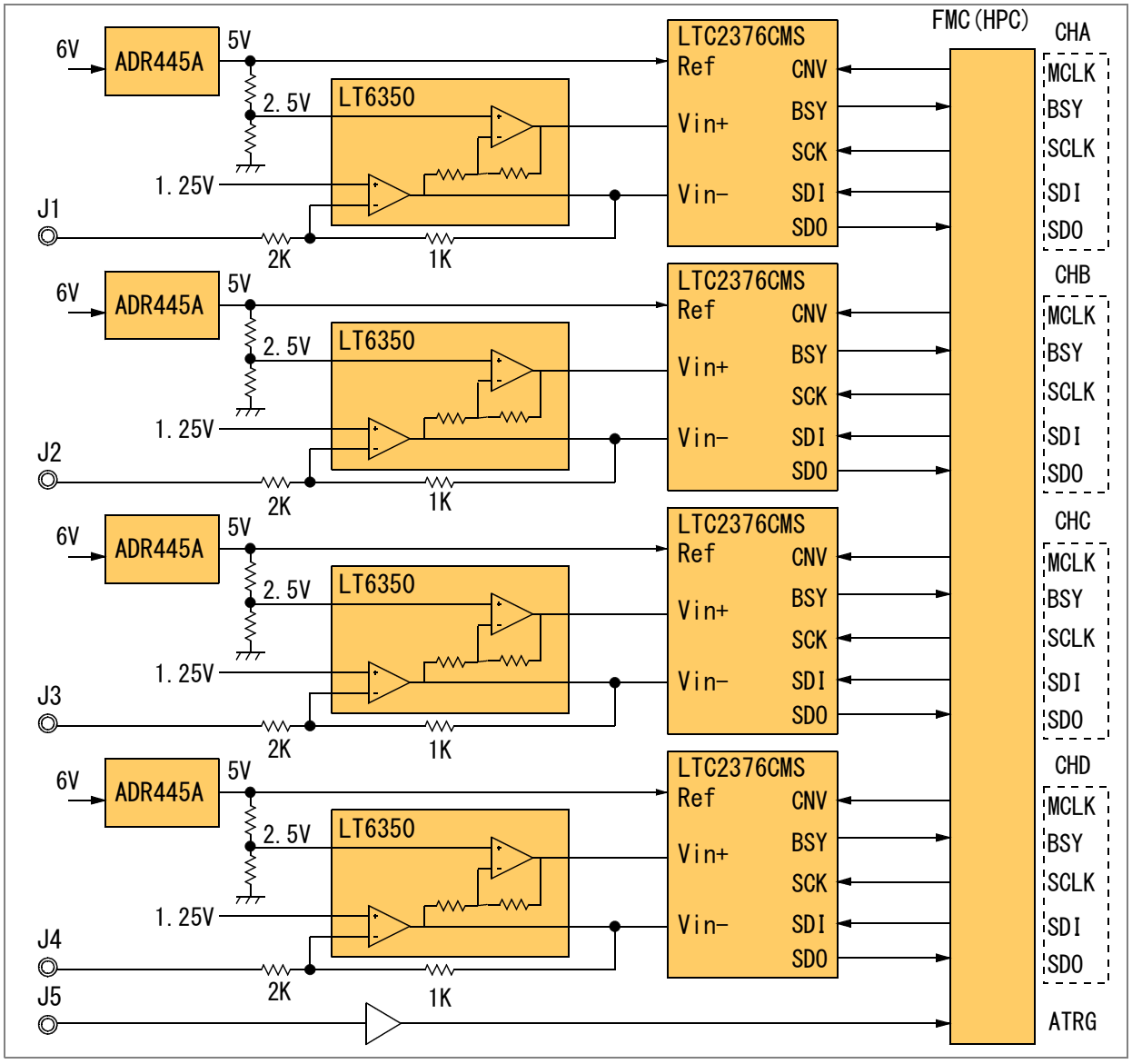

Figure 3-1 Block Diagram

LT1350 are used to convert single ended inputs differential signals, which are input to AD converter (LTC2376-16).

ADC data will be read through SPI on LTC2376CMS.

Please refer data sheet provided by Linear Technology for detail of SPI timing and commands.

4. Board Layout

Figure 4-1 shows the board layout of RFM-ADCFN04-D250KH.

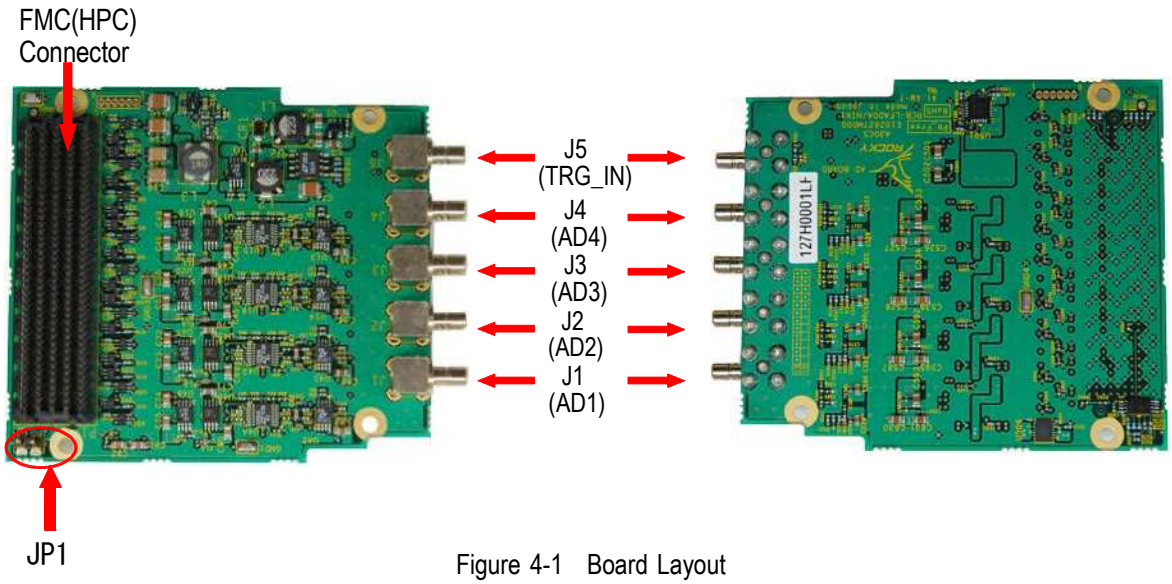

Figure 4-1 Board Layout

Table 4-1 Description of connectors

Item	Description	Remarks
FMC connector	FMC connector (High-Pin Count)	ASP-134488-01 (SAMTEC)
J1～J4	A/D analogue input	414026-3 (Tyco)
J5	Trigger input (LVCMOS_25)	414026-3 (Tyco)
JP1	EEPROM control	HWP-2P-G-M (MAC8)

5. Board Specifications

5.1 Input Signals

Table 5-1 shows the specification of AD input signals.

Table 5-1 specification of DA output signals

Item	Description
Analogue Input	
Number of channels	4 channels
Resolution	16 bits
Maximum Sampling Frequency	250Khz
Coupling	DC coupling
Input Impedance	4Mohm (single ended)
Input level	10Vpp(±5V)
Trigger Input	
Input level	2.5V (LVCMOS)

5.2 Power

Table 5-2 shows input power for the board. All the power are supplied from FMC HPC connector.

Table 5-2 Power

Item	Voltage	Current	Remarks
12P0V	+12V	130 mA (Max)	
3P3V	+3.3V	0.5 mA (Max)	
VADJ	+2.5V	0A	VADJ is only looped back to VIO_M2C
3P3VAUX	+3.3V	3 mA (Max)	

Figure 5-1 shows the block diagram of power distribution.

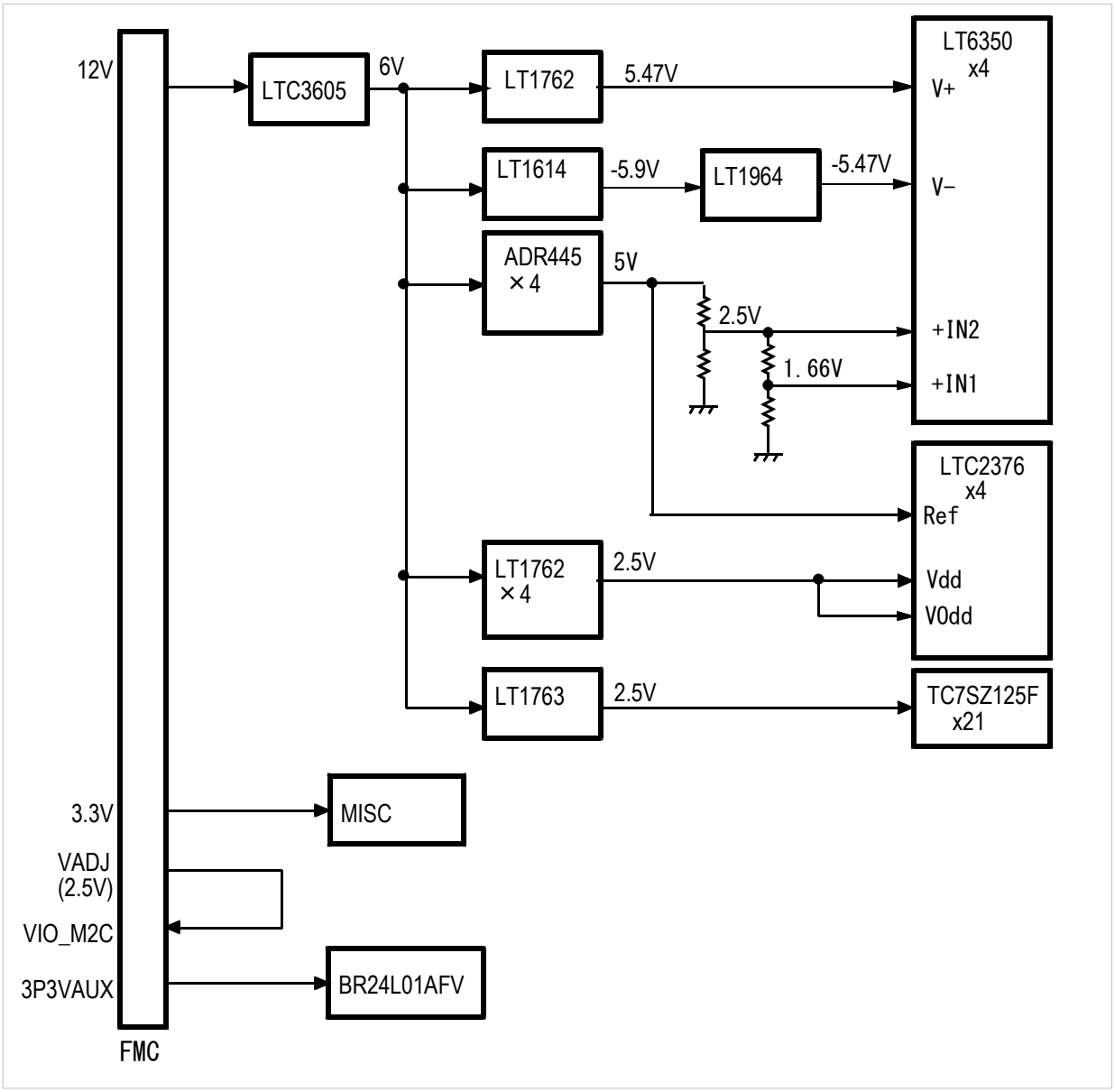

Figure 5-1 Power Distribution

5.3 Jumper

Table 5-2 shows the function of JP1.

Table 5-2 JP1 Function

JP1 Setting	Description
Off	Normal Operation, (Disable to write EEPROM)
On	Set jumper to enable writing EEPROM.

5.4 ADC Circuit

Figure 5-2 shows the outline of the circuit.

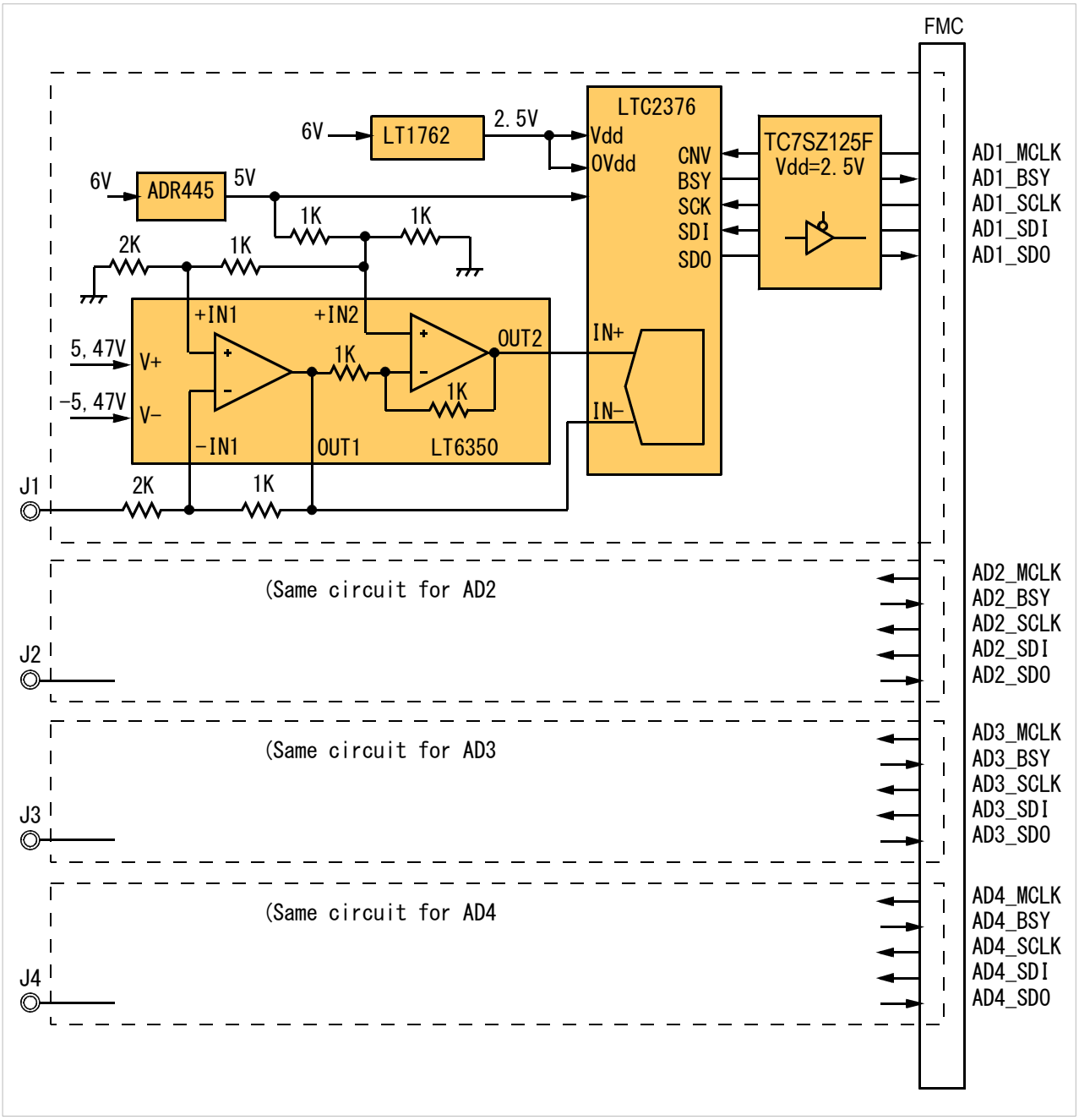

Figure 5-2 Circuit outline

5.5 FMC Connector Pin Assignment

Table 5-3 shows pin assignment of FMC connector.

Table 5.3 Connector Pin Assignment

	K	J	H	G	F	E	D	C	B	A
1	N.C.	GND	N.C.	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND
2	GND	N.C.	PRSNT_M2C_L	CLK1_M2C_P	GND	N.C.	GND	N.C.	GND	N.C.
3	GND	N.C.	GND	CLK1_M2C_N	GND	N.C.	GND	N.C.	GND	N.C.
4	N.C.	GND	N.C.	GND	HA00_P_CC	GND	N.C.	GND	N.C.	GND
5	N.C.	GND	N.C.	GND	N.C.	GND	N.C.	GND	N.C.	GND
6	GND	N.C.	GND	LA00_P_CC	GND	N.C.	GND	N.C.	GND	N.C.
7	N.C.	N.C.	LA02_P	N.C.	N.C.	N.C.	GND	N.C.	GND	N.C.
8	N.C.	GND	LA02_N	GND	N.C.	GND	N.C.	GND	N.C.	GND
9	GND	N.C.	GND	N.C.	GND	N.C.	N.C.	GND	N.C.	GND
10	N.C.	N.C.	LA04_P	N.C.	N.C.	N.C.	GND	N.C.	GND	N.C.
11	N.C.	GND	LA04_N	GND	N.C.	GND	N.C.	N.C.	GND	N.C.
12	GND	N.C.	GND	N.C.	GND	N.C.	N.C.	GND	N.C.	GND
13	N.C.	N.C.	LA07_P	N.C.	N.C.	N.C.	GND	GND	N.C.	GND
14	N.C.	GND	N.C.	GND	N.C.	GND	N.C.	N.C.	GND	N.C.
15	GND	N.C.	GND	N.C.	GND	N.C.	N.C.	N.C.	GND	N.C.
16	N.C.	N.C.	LA11_P	N.C.	N.C.	N.C.	GND	GND	N.C.	GND
17	N.C.	GND	LA11_N	GND	N.C.	GND	N.C.	GND	N.C.	GND
18	GND	N.C.	GND	N.C.	GND	N.C.	N.C.	N.C.	GND	N.C.
19	N.C.	N.C.	LA15_P	N.C.	N.C.	N.C.	GND	N.C.	GND	N.C.
20	N.C.	GND	LA15_N	GND	N.C.	GND	N.C.	GND	N.C.	GND
21	GND	N.C.	GND	N.C.	GND	N.C.	N.C.	GND	N.C.	GND
22	N.C.	N.C.	LA19_P	N.C.	N.C.	N.C.	GND	N.C.	GND	N.C.
23	N.C.	GND	N.C.	GND	N.C.	GND	N.C.	N.C.	GND	N.C.
24	GND	N.C.	GND	N.C.	GND	N.C.	N.C.	GND	N.C.	GND
25	N.C.	N.C.	LA21_P	N.C.	N.C.	N.C.	GND	GND	N.C.	GND
26	N.C.	GND	LA21_N	GND	N.C.	GND	N.C.	N.C.	GND	N.C.
27	GND	N.C.	GND	N.C.	GND	N.C.	N.C.	N.C.	GND	N.C.
28	N.C.	N.C.	LA24_P	N.C.	N.C.	N.C.	GND	GND	N.C.	GND
29	N.C.	GND	LA24_N	GND	N.C.	GND	N.C.	GND	N.C.	GND
30	GND	N.C.	GND	N.C.	GND	N.C.	TDI	SCL	GND	N.C.
31	N.C.	N.C.	LA28_P	N.C.	N.C.	N.C.	TDO	SDA	GND	N.C.
32	N.C.	GND	N.C.	GND	N.C.	GND	3P3VAUX	GND	N.C.	GND
33	GND	N.C.	GND	N.C.	GND	N.C.	N.C.	GND	N.C.	GND
34	N.C.	N.C.	LA30_P	N.C.	N.C.	N.C.	N.C.	GA0	GND	N.C.
35	N.C.	GND	LA30_N	GND	N.C.	GND	GA1	12P0V	GND	N.C.
36	GND	N.C.	GND	LA33_P	GND	N.C.	3P3V	GND	N.C.	GND
37	N.C.	N.C.	N.C.	LA33_N	N.C.	N.C.	GND	12P0V	N.C.	GND
38	N.C.	GND	N.C.	GND	N.C.	GND	3P3V	GND	GND	N.C.
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	N.C.
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	N.C.	GND
	HPC		LPC		HPC		LPC		HPC	

Note: N.C. means #No Connection"

(1) Supply +2.5V to VADJ.
(2) FMC loops back VADJ to VIO_B_M2C.
(3) TDO is looped back from TDI.

Table 5-4 shows the FMC pin assignment of the board.

Table 5-4 The Signal Assignment to FMC connector

Pin#		Signal Name	FMC_LOC	I/O	Description	Remarks	
LTC2376 SPI signal (ADC1)							
G	36	AD1_SCLK	LA33_P	I	ADC SPI clock	LTC2376	SCK
G	37	AD1_SDO	LA33_N	O	ADC SPI data output		SDO
H	34	AD1_SDI	LA30_P	I	ADC SPI datai nput		RDL/SDI
H	35	AD1_BUSY	LA30_N	O	ADC convrtsion indicator		BUSY
H	31	AD1_MCLK	LA20_P	I	ADC initiate conversion		CNV
LTC2376 SPI signal (ADC2)							
H	28	AD2_SCLK	LA24_P	I	ADC SPI clock	LTC2376	SCK
H	29	AD2_SDO	LA24_N	O	ADC SPI data output		SDO
H	25	AD2_SDI	LA21_P	I	ADC SPI datai nput		RDL/SDI
H	26	AD2_BUSY	LA21_N	O	ADC convrtsion indicator		BUSY
H	22	AD2_MCLK	LA19_P	I	ADC initiate conversion		CNV
LTC2376 SPI signal (ADC3)							
H	19	AD3_SCLK	LA15_P	I	ADC SPI clock	LTC2376	SCK
H	20	AD3_SDO	LA15_N	O	ADC SPI data output		SDO
H	16	AD3_SDI	LA11_P	I	ADC SPI datai nput		RDL/SDI
H	17	AD3_BUSY	LA11_N	O	ADC convrtsion indicator		BUSY
H	13	AD3_MCLK	LA07_P	I	ADC initiate conversion		CNV
LTC2376 SPI signal (ADC4)							
H	10	AD4_SCLK	LA04_P	I	ADC SPI clock	LTC2376	SCK
H	11	AD4_SDO	LA04_N	O	ADC SPI data output		SDO
H	7	AD4_SDI	LA02_P	I	ADC SPI datai nput		RDL/SDI
H	8	AD4_BUSY	LA02_N	O	ADC convrtsion indicator		BUSY
G	6	AD4_MCLK	LA00_P_CC	I	ADC initiate conversion		CNV
Other signals							
F	4	ATRG_IN	HA-00_P_CC	I	Trigger Input		
B	1	CLK_DIR	CLK_DIR	O	Clock direction		
C	30	SCL	SCL	I	FMC I2C clock input		
C	31	SDA	SDA	I/O	FMCI2C address/data		
C	34	GA0	GA0	I	FMCI2C address 0	Pulled up to 3P3VAUX	
D	35	GA1	GA1	I	FMCI2C address 1	Pulled up to 3P3VAUX	
D	30	TDI	TDI	I	JTAG data input	looped back to TDO	
D	31	TDO	TDO	O	JTAG data output		
F	1	PG_M2C	PG_M2C	O	Module power good		
G	2	CLK1_M2C_P	CLK1_M2C_P	O	Pulled up to VADJ	Pulled up to VADJ	
G	3	CLK1_M2C_N	CLK1_M2C_N	O	Pulled down to GND	Pulled down to GND	
H	2	PRSNT_M2C_L	PRSNT_M2C_L	O	Module present signal	Pulled down to GND	

6. Operation

(1) Set CNV signal to High. With rising edge of CNV, LTC2376-16 ibitiates conversion.
(2) Check BUSY return to Low, which indicates conversion has finished.
(3) Read out ADC data..

Refer to the LTC2376-16 (Linear Technology) data sheet for detail.

The output data is v2's compliment format.

Input	ADC Data	Remarks
5V－152 μ V	0111 1111 1111 1111	
0V	0000 0000 0000 0000	
－5V	1000 0000 0000 0000	