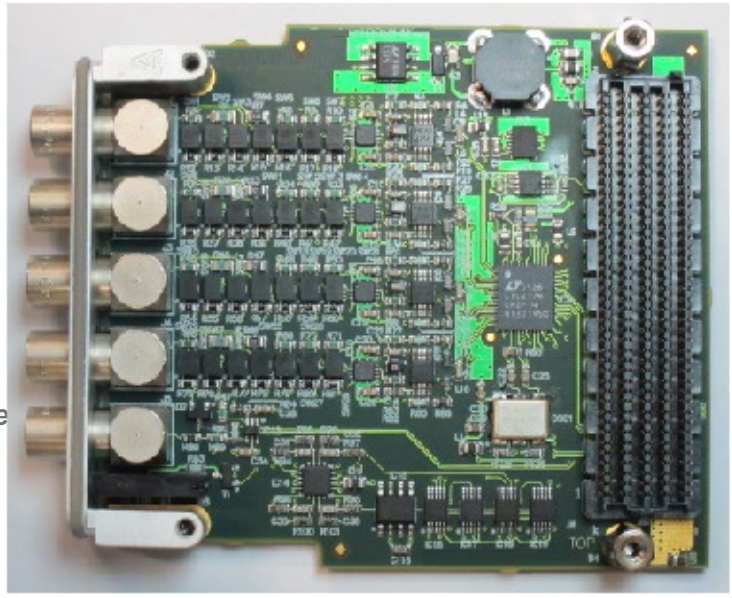
# NES-FMC4ADC FMC Mezzanine module
# 4 channel 100MSPS ADC

## // OVERVIEW

*FMC module  4 channel ADC bits/sample 14 bit (HPC connector)*

*max. sample rate  105 MSPS*

*Analog bandwidth*
*30 MHz. DC-coupled  (40 MHz possible )*



*ENO 11, 11.5, 11.7 bit (@ +/-50mV, +/-0.5V, +/-5V range)*

*connectors*
*4 x LEMO 00 for signals, 1 x LEMO 00 for trigger*

*Input impedance 1 kOhm / 50 Ohm - software selectable*
*offset correction range +/- 5 V for every input*
*voltage rangemax. gain error  +/- 1 %*

*SNR  67.7 dB, 70.8 dB, 72.2 dB (@ +/-50mV, +/-0.5V, +/-5V range)*

*ADC interface  Serial LVDS, 2 pairs for each channel*

## // HIGHLIGHTS

*The NES-FMC4ADC  is a 4 channel 100MSPS 14 bit ADC card in FMC (FPGA Mezzanine Card) format. By default it uses only signals from the LPC rows of the HPC connector that is mounted. The gain can be set by software in three steps: +/-50mV, +/-0.5V, +/-5V. An advanced offset circuit is used in the front-end design of the ADC board, and allows a voltage shift in the range of +/- 5V that is independent on the chosen gain range. To see how this mezzanine can be combined with a carrier and turned into a complete system*