



FMC-CL

(Dual Full/Extended Camera link FMC Module)

User Guide

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REVISION HISTORY

Revision	Comments	Originator	Date
1.0	Initial Release	Stephen Malchi	17 Sep 2016
1.1	Added board pictures and FMC pin mapping	Stephen Malchi	5 Oct 2016



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LIST OF ACRONYMS

CL	Camera Link (AIA Standard 1.2)
FMC	FPGA Mezzanine Card (VITA 57 standard)
FPGA	Field-Programmable Gate Array
MDR	Mini Delta Ribbon (Connector Standard)
MT/s	Mega-transfers per second
P/N	Part Number
PCB	Printed Circuit Board
PoCL	Power Over Camera Link
SATA	Serial AT-Attachment (disk drive interface)
SDR	Shrink Delta Ribbon (connector standard)
VITA	VMEbus International Trade Association



1 INTRODUCTION

FMC-CL is an FMC mezzanine card providing Camera Link and optional SATA interfaces. The board is designed for simplicity and low cost but will still support maximum performance.

1.1 Hardware Features

The hardware has following features:

1. Dual Camera Link Interfaces
2. 7.14 Gb/s on each camera link interface
3. Both interfaces support Base, Medium, Full, Extended Full and dual-Base modes, for a total of four CL connectors
4. Supports pixel clock rate of 85Mhz and higher
5. Quad-Base mode supported
6. Two SDR CL connectors on back panel plus two more off-board CL connectors
7. Each CL interface can be either input or output
8. All CL signals are routed directly to the FMC connector, using pins compatible with the LPC version of FMC for the first CL and with HPC on the second.
9. ESD protection provided on all external pins
10. Power over Camera Link supported on both interfaces, 12V at up to 333mA. PTC fuses on both primary connectors, and each is separately enabled from the FPGA
11. Optional dual SATA connectors for direct disk interface.

1.2 Applicable Specifications

The board is compliant with both of the following specifications:

1. ANSI/VITA 57.1A FMC
2. AIA Camera Link 1.2

2 BOARD DESCRIPTION

2.1 Block Diagram

The following diagram shows the major blocks of FMC-CL:

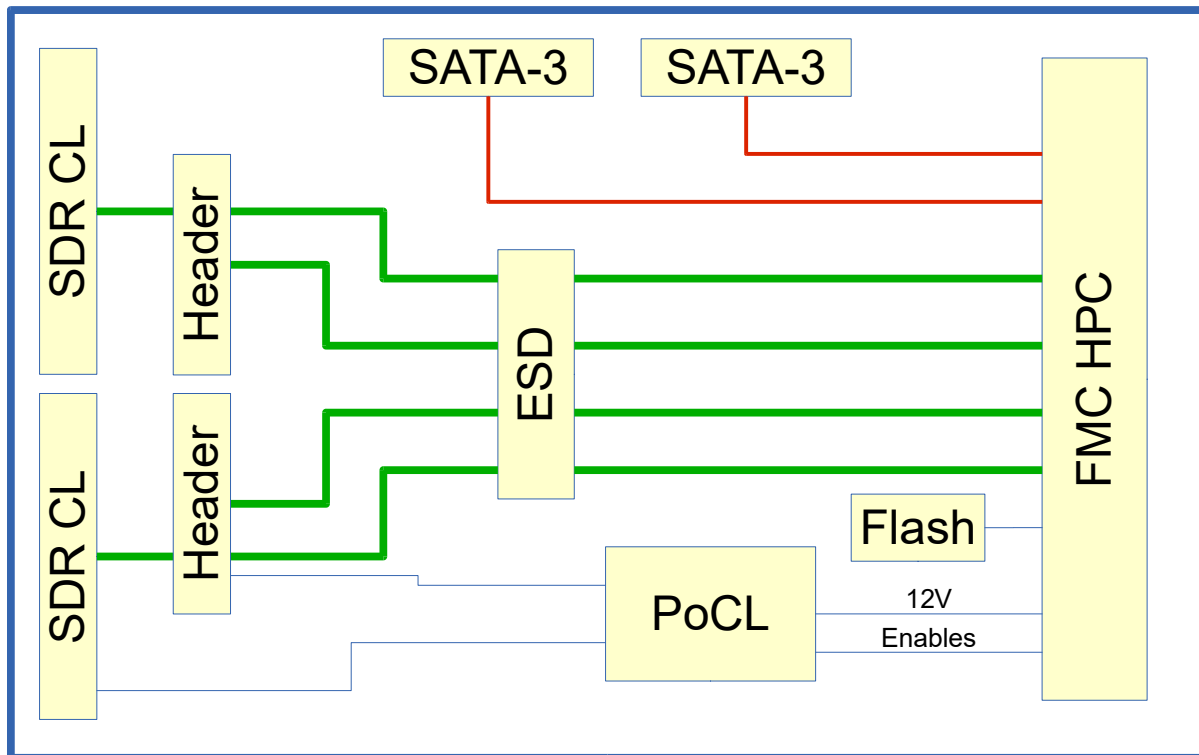


Figure 1 - Block Diagram

2.2 Images of FMC Module and Auxiliary IO card

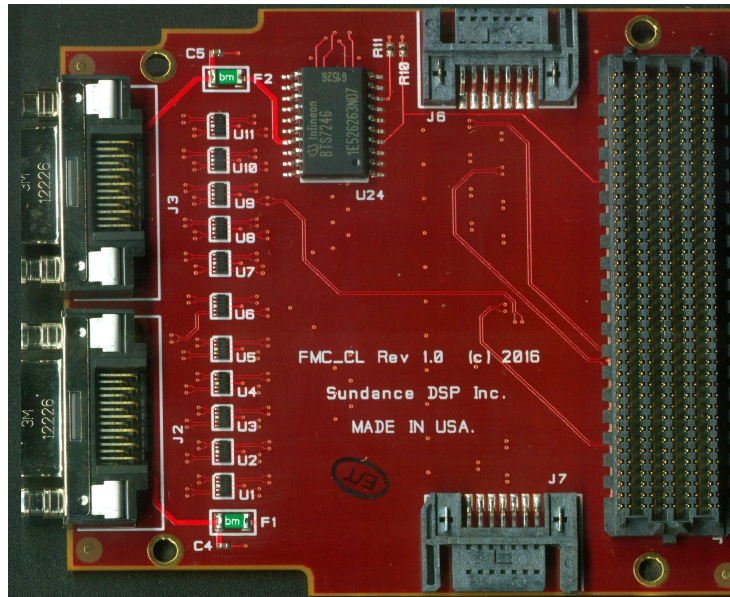


Figure 2 - Component side of FMC Module

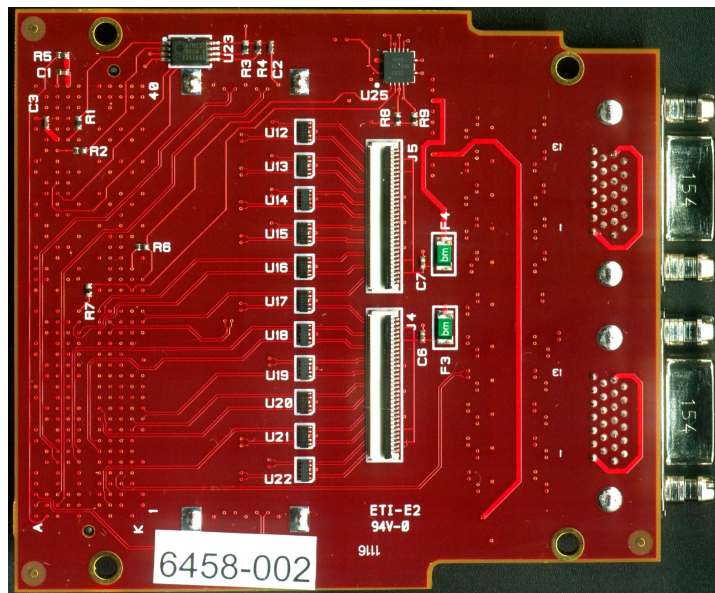


Figure 3 - Solder side of FMC Module



Figure 4 - FMC and Auxiliary PC card side by side

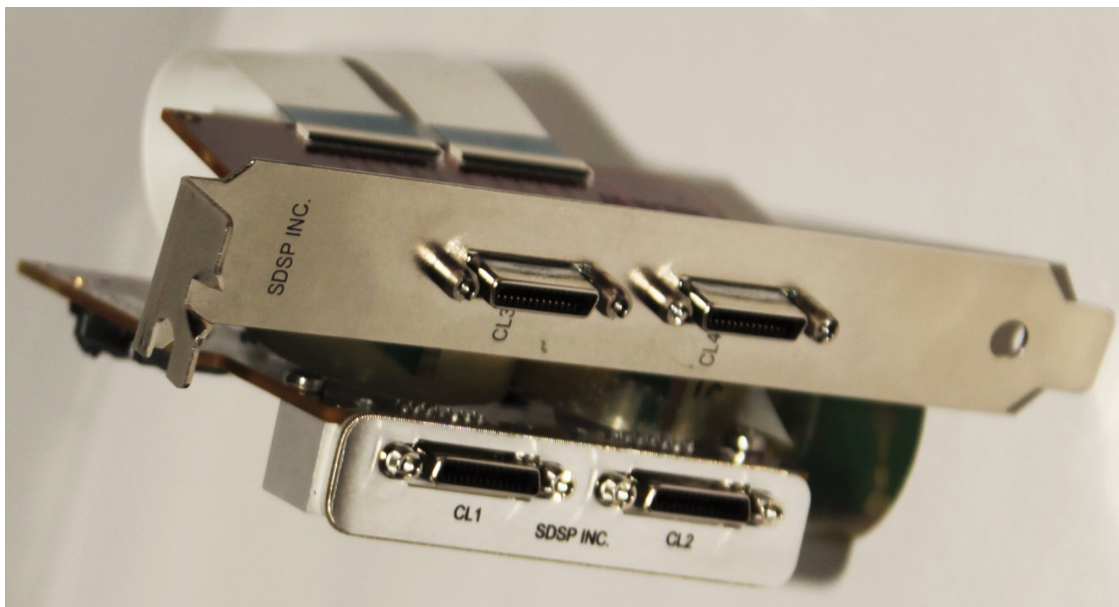


Figure 5 - Image showing FMC and Auxiliary card connected via flat cable

2.3 FMC HPC

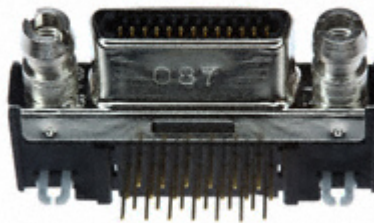
Each CL connector or header has 11 differential LVDS pairs (allowing for dual base mode on each CL pair), two grounds, and two pins used for PoCL or ground. The FMC spec provides up to 34 pairs plus two clock pairs on the LPC version, so all 44 pairs cannot be implemented within LPC. The first CL, first SATA, and all PoCL control pins are taken to the LPC rows (LA_xx and DP0). The second CL interface (through the headers) is implemented via the HA pins on the HPC rows (HA_xx and DP1).

2.4 Clocking

Each full CL link requires three LVDS clock inputs, for a total of six clocks when both interfaces are used. VITA 57.1 provides two dedicated clocks CLK0_M2C and CLK1_M2C, plus three or four “clock capable” pairs in each signal group. The dedicated clocks are used for the base CL input on each CL pair (one back panel, one header), and the medium / full clocks are routed to the LA00_CC, LA01_CC and HA00_CC, HA01_CC FMC pins.

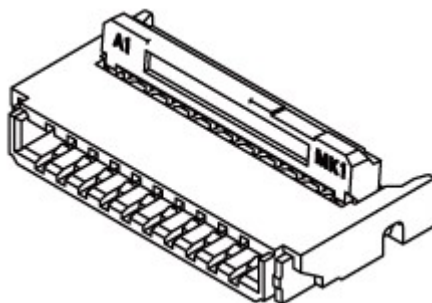
2.5 Camera Link Connector, Back Panel

The back-panel camera link connector is a 26-pin SDR type, such as 3M P/N [12226-5150-00FR](#). This connector is through-hole for mechanical strength.



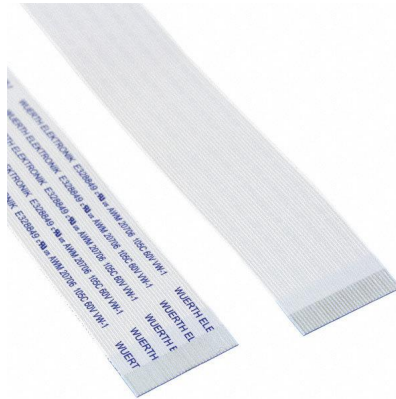
2.6 Off-board Headers

The off-board headers are 0.5mm 32 pin back flip FPC connector right-angle surface mount headers (Molex part number [50348032](#)). These two headers are placed on solder side of the FMC where there is 2.9mm of clearance for the cables.



2.7 Flat Flex cables

32 position flat flex cables are used to connect the FMC to the second Camera link IO card, Part number [152660343](#).



2.8 SATA Connectors

Two SATA connectors are placed closed to the FMC connector on the component side, to allow right-angle cables to be connected to the disk drives. .

The first SATA lane is connected to LPC DP0_C2M and DP0_M2C, the second lane is connected to HPC DP1_C2M and DP1_M2C.

2.9 ESD Protection

ESD protection is provided by Semtech RClamp0524P component intended for use with high speed LVDS signals (>600MHz) with minimum impact on signal quality.

2.10 Power over Camera Link

PoCL support is provided from 12V input to the FMC, with PTC resettable fuses on each connector. Fuses will pass 0.333 A over the operating temperature of the board with the lowest reasonable trip point above that. Each PoCL link is enabled only by active input from the FPGA, with pull-up/down provided by resistor to guarantee no power applied before the FPGA is configured.

Note: In order to enable the PoCL on a Camera link connector set the enable pin to logic high inside the FPGA.



2.11 Flash Memory

A small on-board I2C flash memory is provided for identification and power requirement information to the carrier.



3 OPERATION

This section describes how to install the hardware and initialize various devices on FMC_CL.

3.1 Carrier/Motherboard

FMC-CL is a daughter card with HPC FMC and can be populated on carrier cards with both LPC and HPC FMC connectors.

3.2 Power Supplies

FMC-CL conforms to FMC standard. However only two voltages are used on the card. These voltages are brought to the card through the FMC connector. The voltages are used as follows:

1. 3.3_AUX : For powering EEPROM
2. 12v : For PoCL

3.3 VADJ voltage

The module only uses VADJ voltage for level translation of PoCL enable pins from VADJ to 3.3v. Other than that it not used on the card.

Note: The VADJ voltage on the carrier card should be selected based on the LVDS signalling provided in the camera's user guide.

3.4 Firmware IP Core

As mentioned earlier this is a simple FMC card where all the serial channels (LVDS signals) are taken from the camera link connectors and Off-board headers to the FMC connector. Therefore the de-serialization is done in the FPGA.

The IP core is based on the de-serialization primitives in the FPGA which depends on the family and vendor used. As of now Sundance DSP has IP core supported on Xilinx 7-series and Ultrascale FPGA's.

Note: Please contact Sundance DSP for license and pricing information.



4 APPENDIX

4.1 Pinout

4.1.1 FMC HPC

FMC-CL HPC Pinout (J1 Connector)										
S.No	Row A	Row B	Row C	Row D	Row E	Row F	Row G	Row H	Row J	Row K
1	GND	NC	GND	NC	GND	NC	GND	NC	GND	NC
2	SATA_B_RX+	GND	SATA_A_TX+	GND	CL_B_ZCLK+	GND	CL_B_XCLK+	GND	NC	GND
3	SATA_B_RX-	GND	SATA_A_TX-	GND	CL_B_ZCLK-	GND	CL_B_XCLK-	GND	NC	GND
4	GND	NC	GND	NC	GND	CL_B_YCLK+	GND	CL_A_XCLK+	GND	NC
5	GND	NC	GND	NC	GND	CL_B_YCLK-	GND	CL_A_XCLK-	GND	NC
6	NC	GND	SATA_A_RX+	GND	CL_B_CC3+	GND	CL_A_YCLK+	GND	CL_B_CC1+	GND
7	NC	GND	SATA_A_RX-	GND	CL_B_CC3-	CL_B_CC2+	CL_A_YCLK-	CL_A_CC4+	CL_B_CC1-	CL_B_CC4+
8	GND	NC	GND	CL_A_ZCLK+	GND	CL_B_CC2-	GND	CL_A_CC4-	GND	CL_B_CC4-
9	GND	NC	GND	CL_A_ZCLK-	CL_B_X2+	GND	CL_A_CC3+	GND	CL_B_SERTC+	GND
10	NC	GND	CL_A_SERTFG+	GND	CL_B_X2-	CL_B_X3+	CL_A_CC3-	CL_A_CC2+	CL_B_SERTC-	CL_B_SERTFG+
11	NC	GND	CL_A_SERTFG-	CL_A_CC1+	GND	CL_B_X3-	GND	CL_A_CC2-	GND	CL_B_SERTFG-
12	GND	NC	GND	CL_A_CC1-	NC	GND	CL_A_X3+	GND	CL_B_X0+	GND
13	GND	NC	GND	GND	NC	CL_B_RSVD+	CL_A_X3-	CL_A_SERTC+	CL_B_X0-	CL_B_X1+
14	NC	GND	CL_A_X1+	CL_A_X2+	GND	CL_B_RSVD-	GND	CL_A_SERTC-	GND	CL_B_X1-
15	NC	GND	CL_A_X1-	CL_A_X2-	CL_B_Z2+	GND	CL_A_Z3+	GND	CL_B_Z1+	GND
16	GND	NC	GND	GND	CL_B_Z2-	CL_B_Z0+	CL_A_Z3-	CL_A_X0+	CL_B_Z1-	CL_B_Z3+
17	GND	NC	GND	CL_A_Z2+	GND	CL_B_Z0-	GND	CL_A_X0-	GND	CL_B_Z3-
18	NC	GND	CL_A_Z1+	CL_A_Z2-	CL_B_Y1+	GND	CL_A_RSVD+	GND	CL_B_Y3+	GND
19	NC	GND	CL_A_Z1-	GND	CL_B_Y1-	CL_B_Y2+	CL_A_RSVD-	CL_A_Z0+	CL_B_Y3-	CL_B_Y0+
20	GND	NC	GND	NC	GND	CL_B_Y2-	GND	CL_A_Z0-	GND	CL_B_Y0-
21	GND	NC	GND	NC	NC	GND	CL_A_Y2+	GND	PoCL_EN_B_1	GND
22	SATA_B_TX+	GND	NC	GND	NC	NC	CL_A_Y2-	CL_A_Y3+	STATUS_3_4	PoCL_EN_B_2
23	SATA_B_TX-	GND	NC	PoCL_EN_A_1	GND	NC	GND	CL_A_Y3-	GND	NC
24	GND	NC	GND	STATUS_1_2	NC	GND	CL_A_Y0+	GND	NC	GND
25	GND	NC	GND	GND	NC	NC	CL_A_Y0-	CL_A_Y1+	NC	NC
26	NC	GND	NC	NC	GND	NC	GND	CL_A_Y1-	GND	NC
27	NC	GND	NC	NC	NC	GND	NC	GND	NC	GND
28	GND	NC	GND	GND	NC	NC	NC	PoCL_EN_A_2	NC	NC
29	GND	NC	GND	NC	GND	NC	GND	NC	GND	NC
30	NC	GND	FMC_I2C_SCL	FMC_TDI_BUF	NC	GND	NC	GND	NC	GND
31	NC	GND	FMC_I2C_SDA	FMC_TDO_BUF	NC	NC	NC	NC	NC	NC
32	GND	NC	GND	V3P3_AUX	GND	NC	GND	NC	GND	NC
33	GND	NC	GND	NC	NC	GND	NC	GND	NC	GND
34	NC	GND	FMC_GA0	FMC_GA1	NC	NC	NC	NC	NC	NC
35	NC	GND	V12P0	GND	GND	NC	GND	NC	GND	NC
36	GND	NC	GND	V3P3	NC	GND	NC	GND	NC	GND
37	GND	NC	V12P0	GND	NC	NC	NC	NC	NC	NC
38	NC	GND	GND	V3P3	GND	NC	GND	NC	GND	NC
39	NC	GND	V3P3	GND	VADJ	GND	VADJ	GND	NC	GND
40	GND	NC	GND	V3P3	GND	VADJ	GND	VADJ	GND	NC

Figure 6 - FMC-CL Pinout

Note: FMC_TDI_BUF and FMC_TDO_BUF pins are shorted on FMC_CL as per ANSI/VITA 57.1 FMC Standard Rule 5.62



4.2 Camera Link and FMC Pin Mapping

FMC-CL can be used both as a frame grabber and as a camera link simulator.

Note: As of now only the input mapping is tested and provided below.

4.2.1 Camera Link A (Base connector)

Signal Name	FMC Pin	FMC Signal	SDR (J2)
X0_P	H16	LA11_P	12
X0_N	H17	LA11_N	25
X1_P	C14	LA10_P	11
X1_N	C15	LA10_N	24
X2_P	D14	LA09_P	10
X2_N	D15	LA09_N	23
XCLK_P	H4	CLK0_M2C_P	9
XCLK_N	H5	CLK0_M2C_N	22
X3_P	G12	LA08_P	8
X3_N	G13	LA08_N	21
SERTC_P	H13	LA07_P	20
SERTC_N	H14	LA07_N	7
SERTFG_P	C10	LA06_P	6
SERTFG_N	C11	LA06_N	19
CC1_P	D11	LA05_P	5
CC1_N	D12	LA05_N	18
CC2_P	H10	LA04_P	17
CC2_N	H11	LA04_N	4
CC3_P	G9	LA03_P	3
CC3_N	G10	LA03_N	16
CC4_P	H7	LA02_P	15
CC4_N	H8	LA02_N	2
PoCL_J2			1,26
GND			13,14

Table 1 - Camera Link A (Base Connector)

4.2.2 Camera Link A (Medium/Full Connector)

Signal Name	FMC Pin	FMC Signal	SDR (J3)
Y0_P	G24	LA22_P	12
Y0_N	G25	LA22_N	25
Y1_P	H25	LA21_P	11
Y1_N	H26	LA21_N	24
Y2_P	G21	LA20_P	10
Y2_N	G22	LA20_N	23
YCLK_P	G6	LA00_P_CC	9
YCLK_N	G7	LA00_N_CC	22
Y3_P	H22	LA19_P	8
Y3_N	H23	LA19_N	21
RSVD_P	G18	LA16_P	20
RSVD_N	G19	LA16_N	7
Z0_P	H19	LA15_P	6
Z0_N	H20	LA15_N	19
Z1_P	C18	LA14_P	5
Z1_N	C19	LA14_N	18
Z2_P	D17	LA13_P	4
Z2_N	D18	LA13_N	17
ZCLK_P	D8	LA01_P_CC	3
ZCLK_N	D9	LA01_N_CC	16
Z3_P	G15	LA12_P	2
Z3_N	G16	LA12_N	15
PoCL_J3			1,26
GND			13,14

Table 2 - Camera Link A (Medium/Full Connector)



4.2.3 Camera Link B (Base Connector)

Signal Name	FMC Pin	FMC Signal	SDR (J4)
X0_P	J12	HA11_P	12
X0_N	J13	HA11_N	25
X1_P	K13	HA10_P	11
X1_N	K14	HA10_N	24
X2_P	E9	HA09_P	10
X2_N	E10	HA09_N	23
XCLK_P	G2	CLK1_M2C_P	9
XCLK_N	G3	CLK1_M2C_N	22
X3_P	F10	HA08_P	8
X3_N	F11	HA08_N	21
SERTC_P	J9	HA07_P	20
SERTC_N	J10	HA07_N	7
SERTFG_P	K10	HA06_P	6
SERTFG_N	K11	HA06_N	19
CC1_P	J6	HA03_P	5
CC1_N	J7	HA03_N	18
CC2_P	F7	HA04_P	17
CC2_N	F8	HA04_N	4
CC3_P	E6	HA05_P	3
CC3_N	E7	HA05_N	16
CC4_P	K7	HA06_P	15
CC4_N	K8	HA06_N	2
PoCL_J4			1,26
GND			13,14

Table 3 - Camera Link B (Base Connector)



4.2.4 Camera Link B (Medium/Full Connector)

Signal Name	FMC Pin	FMC Signal	SDR (J5)
Y0_P	K19	HA21_P	12
Y0_N	K20	HA21_N	25
Y1_P	E18	HA20_P	11
Y1_N	E19	HA20_N	24
Y2_P	F19	HA19_P	10
Y2_N	F20	HA19_N	23
YCLK_P	F4	HA00_P_CC	9
YCLK_N	F5	HA00_N_CC	22
Y3_P	J18	HA18_P	8
Y3_N	J19	HA18_N	21
RSVD_P	F13	HA12_P	20
RSVD_N	F14	HA12_N	7
Z0_P	F16	HA15_P	6
Z0_N	F17	HA15_N	19
Z1_P	J15	HA14_P	5
Z1_N	J16	HA14_N	18
Z2_P	E15	HA16_P	4
Z2_N	E16	HA16_N	17
ZCLK_P	E2	HA01_P_CC	3
ZCLK_N	E3	HA01_N_CC	16
Z3_P	K16	HA17_P_CC	2
Z3_N	K17	HA17_N_CC	15
PoCL_J5			1,26
GND			13,14

Table 4 - Camera Link B (Medium/Full Connector)



4.3 PoCL Enable FMC Pin Mapping

Signal Name	FMC Pin	FMC Signal
PoCL_EN_J2	D23	LA23_P
PoCL_EN_J3	H28	LA24_P
PoCL_EN_J4	J21	HA22_P
PoCL_EN_J5	K22	HA23_P
STATUS_J2/J3	D24	LA23_N
STATUS_J4/J5	J22	HA22_N

Table 5 - PoCL Enable Pin Mapping

4.4 SATA FMC Pin Mapping

Signal Name	FMC Pin	FMC Signal
SATA_A_TX+	C2	DP0_C2M_P
SATA_A_TX-	C3	DP0_C2M_N
SATA_A_RX+	C6	DP0_M2C_P
SATA_A_RX-	C7	DP0_M2C_N
SATA_B_TX+	A22	DP1_C2M_P
SATA_B_TX-	A23	DP1_C2M_N
SATA_B_RX+	A2	DP1_M2C_P
SATA_B_RX-	A3	DP1_M2C_N

Table 6 - SATA Pin Mapping