FMC-DAQ2p5 ADC/DAC Module

User Guide

REVISION HISTORY

Revision	Comments	Originator	Date
1.0	draft	Nory Nakhaee	Nov, 4th 2016

TABLE OF CONTENTS

1 INTRODUCTION

This document provides information on how to install and use the FMC-DAQ2p5 module (referred to as "the module"). The module is a high pin count FMC (HPC) with one channel of 2.7GSPS 12-bit ADC, and 2.8GSPS dual channel with 16bit resolution. Both interfaces use JESD204B IP core from Xilinx or other third parties.

1.1 Hardware features

The hardware has the following features:
1. ADC12J2700 – 12bit 2.7GSPS JESD204B.
2. LM95233 for ADC temperature monitoring.
3. JESD204B via HPC connector, 8 lanes 5.4Gbps per lane.
4. AD9136 – 16-bit dual channel 2.8GSPS JESD204B DAC.
5. HMC7044 – High performance 3.2GHz JESD204B jitter attenuator.
6. 5x SSMC connectors for:
7. One single ended input for ADC signal, up to 2.7GHz.
   - One for trigger input (logic level).
   - One for clock input (can be used as Device clock for ADC and DAC, and can be used as reference clock for ADC and DAC)
   - 2 output connectors for DAC output, type SSMC.
8. JESD204B Subclass 1 capable.
9. 100 MHz onboard VCXO.
10. 2 Tx and Rx High speed lanes available on Molex nano-pitch connector accessible at the bezzel.
11. 2 Additional LVDS lines from FMC connector available via Molex nano-pitch connector.
12. 2 Clock signals and Vadj power supply available on Molex nano-pitch connector.
13. I2C from FMC connector available via Molex nano-pitch connector.
14. Vadj supported voltages:1.8V, 2.5V, 3.3V
15. Power consumptions: 12V – max 1.1A, 3.3V – max 0.6A, Vadj – max 0.1A

1.2 Board limitations and notes.

1. Maximum line rate for DAC is 10.6 Gb/s, so you must be sure that FPGA board transceivers, can support this rate.
2. When using internal VCXO maximum ADC sample rate is 2.6 GSPS, and maximum DAC speed is 2.08 GSPS, when working simultaneously.
3. When using with PXIe700 FPGA board, GTX speed maximum 8Gb/s, so DAC speed is limited to 1.56 GSPS, when in single mode, or 1.3 GSPS with ADC running on 2.6 GSPS.
4. External input clock limited to 4 GHz.
5. ADC minimum input frequency is 30 MHz.
6. DAC minimum output frequency is 20 MHz.

1.3 FMC-DAQ2p5 board Block Diagram

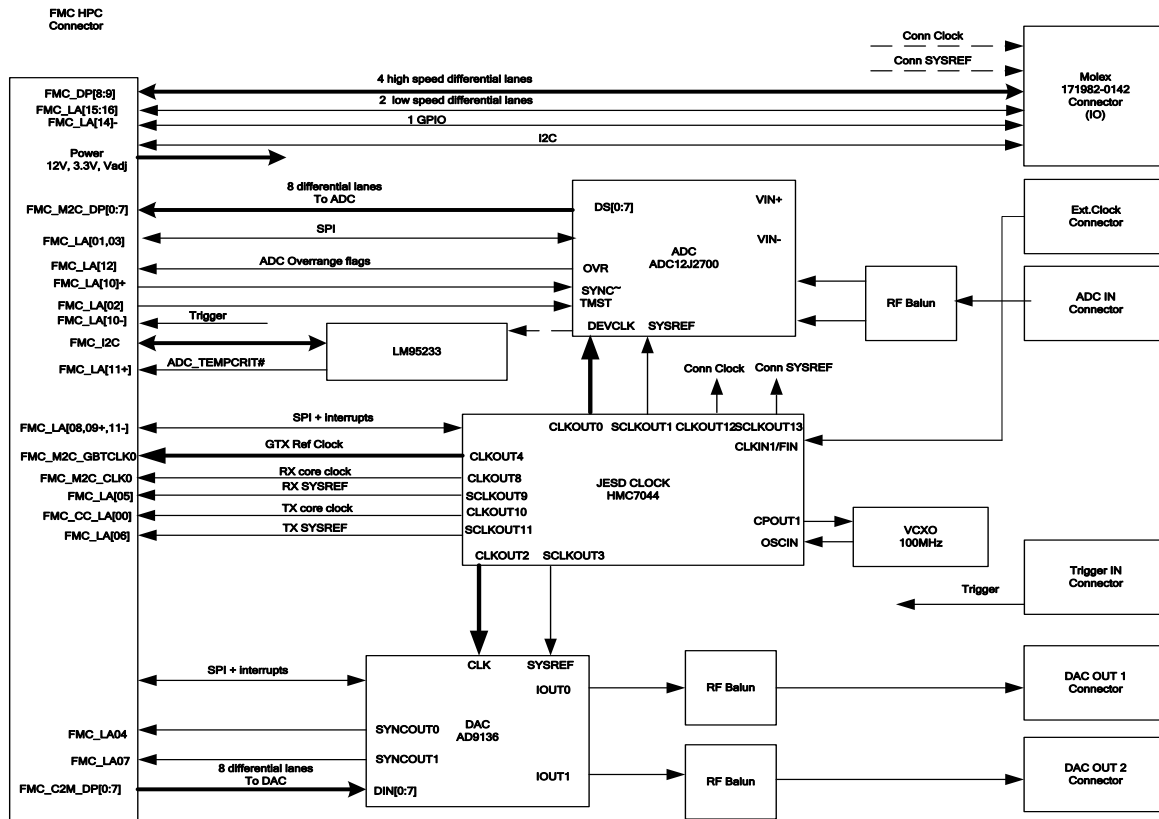The following diagram shows the major blocks of FMC-DAQ2p5 board:

Figure 1: FMC-DAQ2p5 board Block Diagram

2 DESCRIPTION

In this section a brief description of the working of the main functional features is provided.

The main clock distribution IC on this module is HMC7044 from ADI. This IC has multiple clock outputs with SYSREF clock, and provides possibility to clock JESD204B devices.
The module is fitted with 1 ADC12J2700 IC for 1 channel of ADC and the AD9136 to provide 2 channels of DAC. These devices are both JSD204B complaint. They can work with various sample rates; there is also a possibility to enable decimation for ADC and interpolation for DAC. For details of these devices please refer to their respective manuals, and for your reference links to the main ICs' reference guides is included at the end of this document section 6.

External trigger input on this module allows users to add a time stamps on the sample stream from ADC.

CLK IN interface can be a Sample clock input up to 4GHz, or reference clock input up to 1GHz. Board clocking structure provides the possibility of deterministic latency and subclass 1 synchronization.

Simultaneous operation of ADC and DAC is supported at a sample rate of 2.1GSPS, using internal VCXO clock. In this case clocks from 2.1GHz clocks from HMC7044 goes to ADC and DAC. This IC also provides SYSREF clock with known and adjustable delay. Per JESD204B, REF and SYSREF CLK are provided to FPGA to achieve requirement of subclass 1 JESD204B.
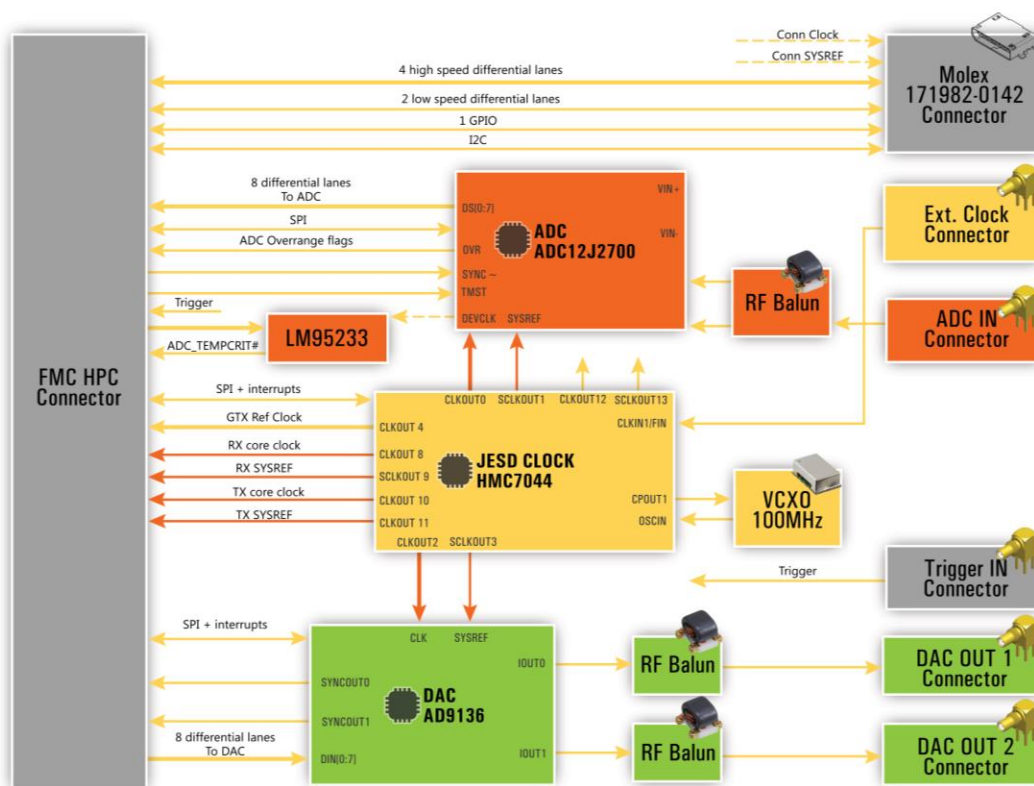
Figure 2: Simplified FMC-DAQ2p5 board Block Diagram

In the FPGA, REF CLK can be used to clock TX and RX paths. Inside the FPGA transceivers there are two PLLs. One QPLL – common for four transceivers (called quad), and CPLL – one for each transceiver. These provide possibility to run Rx and Tx channels at different rates. For more information see **PG066-JESD204.pdf** from Xilinx. See sections on Sharing Transceivers between Transmit and Receive.

3 CLOCK PROGRAMMING GUIDE

To achieve maximum data throughput from ADC and DAC during simultaneous operation, user must program the clock chips as detailed below.

HMC7044 VCO frequency must be set to 2.6GHz. Device clock to ADC must be set to 2.6GHz, setting channel divider to 1.

Per ADC datasheet line rate will be 2*Fs = 5.2 Gb/s and using 8 lanes. This requires a 5200/40 = 130 MHz clock for JESD204 Rx core, this can be achieved by programming output channel divider to 20.

Device Clock to DAC must be 260MHz, this is achieved by programming channel divider in the HMC7044 to 10. Inside DAC you must turn on DAC PLL, and set following parameters: RefDivFactor = 4(REF_DIV_MODE register = 2), LODivFactor = 4(LO_DIV_MODE register = 1), BCount = 16. This give us DAC sample rate of 2080 MHz and 10.4Gb/s Lane rate with 8 lanes. This requires 10400/40 = 260 MHz for JESD Tx Core, and is achieved by programming output channel divider of HMC7044 to 10.

This is the proposed method for achieving 2.6GSPS for ADC and 2.08GSPS for DAC. Many other combinations of frequencies are available and please see datasheet in the references.

3.1 Programming to maximum rates with PXIe_700 board.

A complete Vivado project using this module with Sundance DSP's PXIe700 is provided to kick start the development. For using the module on the PXI700 the HMC7044 VCO frequency must be set to 2.6GHz. Device clock to ADC must be set to 2.6GHz, setting channel divider to 1.

According to ADC datasheet line rate will be 2*Fs = 5.2 Gb/s and using 8 lanes. This requires a 5200/40 = 130 MHz clock for JESD204 Rx core, this can be achieved by programming output channel divider to 20.

Device Clock to DAC must be set to 260MHz, and this is achieved by programming channel divider in the HMC7044 to 10. Inside DAC you must turn on DAC PLL, and set following parameters: RefDivFactor = 4(REF_DIV_MODE register = 2), LODivFactor = 4(LO_DIV_MODE register = 1), BCount = 10. This give us DAC sample rate 1300 MHz and 6.5Gb/s Lane rate with 8 lanes. This requires 6500/40 = 162.5 MHz for JESD Tx Core, and is achieved by programming output channel divider of HMC7044 to 16.

By using the above settings 2.6GSP/S for ADC and 1.33GSP/S for DAC is achieved. Again, there are a lot of other combinations of available frequencies which can be achieved by changing the settings.

4 MAIN PARAMETERS OF THE FMC-DAQ2P5 BOARD

4.1 ADC part parameters

12-Bit Resolution, single-Chanel, 2.7-GSPS ADC
Noise Floor: –146 dBFS/Hz

INL: ±2 LSB (Ta = 25)
DNL: ±0.25 LSB (Ta = 25)
Spectral Performance (f_{IN} = 600 MHz at –1 dBFS):
SNR: 54.8 dBFS
NSD: –146 dBFS/Hz
SFDR: 71.6 dBFS
ENOB: 8.8 Bits
Spectral Performance (f_{IN} = 1500 MHz at –1 dBFS):
SNR: 52.5 dBFS
SFDR: 65.2 dBFS
THD: -68 dBFS
Input Full-Scale differential: 0.95 V_{PP}
Full power Bandwidth (-3 dB – calibration = FG): 3200 MHz
Integrated Wideband DDC Block
Input type: AC – coupled, single ended.
Input frequency range: 30 – 1800 MHz
Maximum input voltage – 2 Vpp single ended
Power Dissipation: 2.21 W max at 2.7 GSPS

4.2 DAC part parameters

Resolution: 16-Bit
Maximum Sample Rate: 2.8GSPS
Maximum Input Data Rate: 2.12GSPS
8 JESD204B Serial Input Lanes
10.6 Gbps Maximum Bit Rate per Lane
Subclass 1 -DAC Synchronization
On-Chip Very Low Jitter PLL
Selectable 1x –8x Interpolation
Sinx/x Correction Filters
3/4-Wire Serial Control Bus (SPI)
Outputs: AC coupled, transformer isolated
Output voltage range: 2Vpp max
Output frequency range: 20 – 1060 MHz
Integrated Temperature Sensor
Power Dissipation: 1.74W at 1.6GSPS

4.3 Clock and trigger in parameters

- External clock in frequency range, in reference clock mode – 10 – 800MHz
- External clock in frequency range, in device clock mode – 400 – 4000MHz
- Input: AC coupled, 50 Ohm, single ended.
- Input power range: -6 to 6 dBm.
- Trigger input – logic level, ESD protected, LVTTL 3.3V

4.4 Pictures of the Module
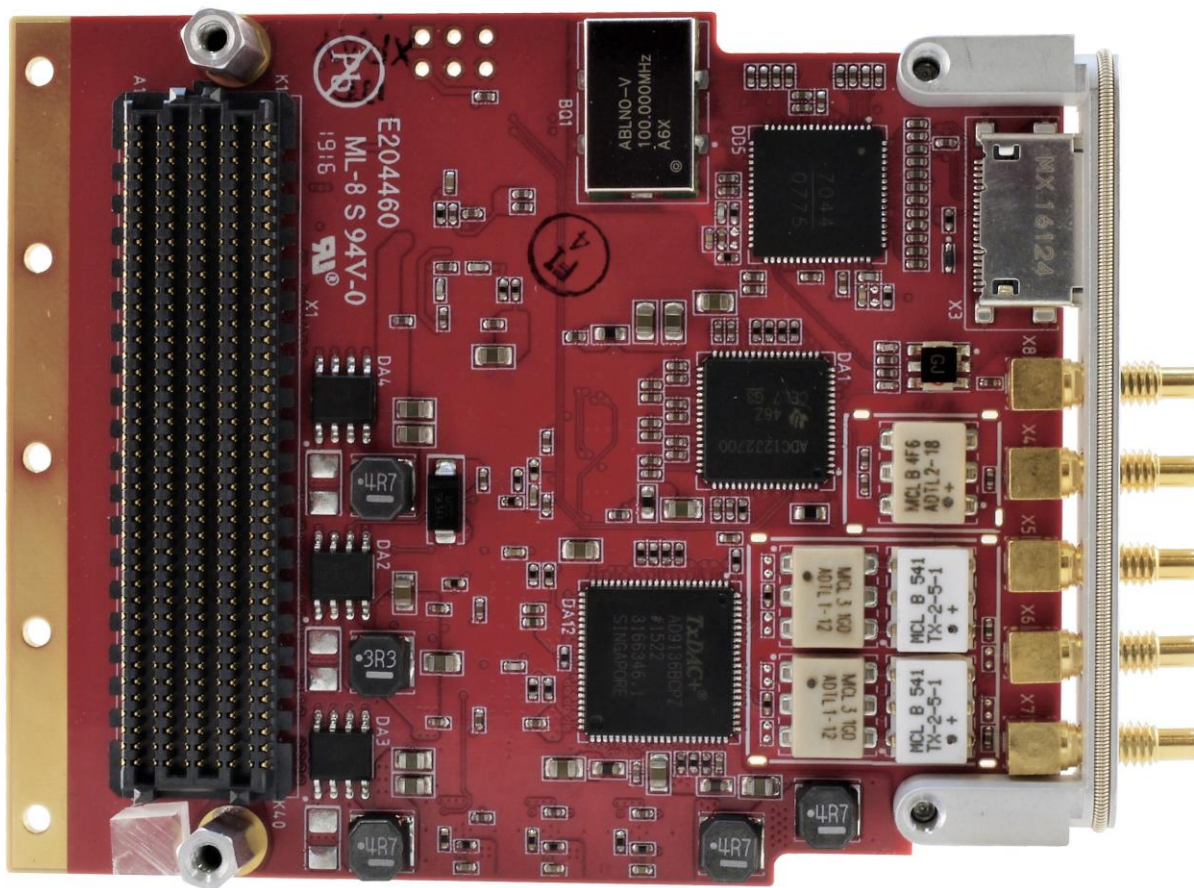
Component side of FMC-DAQ2p5
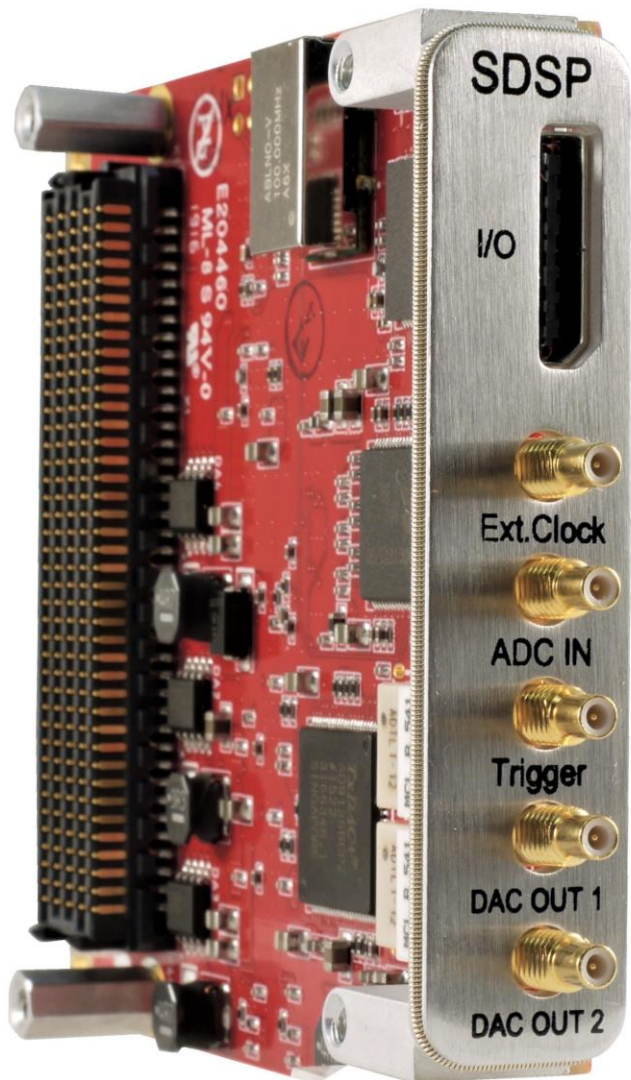
Side/frontal view of FMC-DAQ2p5

A 3D view of the Module can be seen here (open hyperlink)

5 PINOUTs

5.1 Pinout for HPC connector of FMC-DAQ2p5.

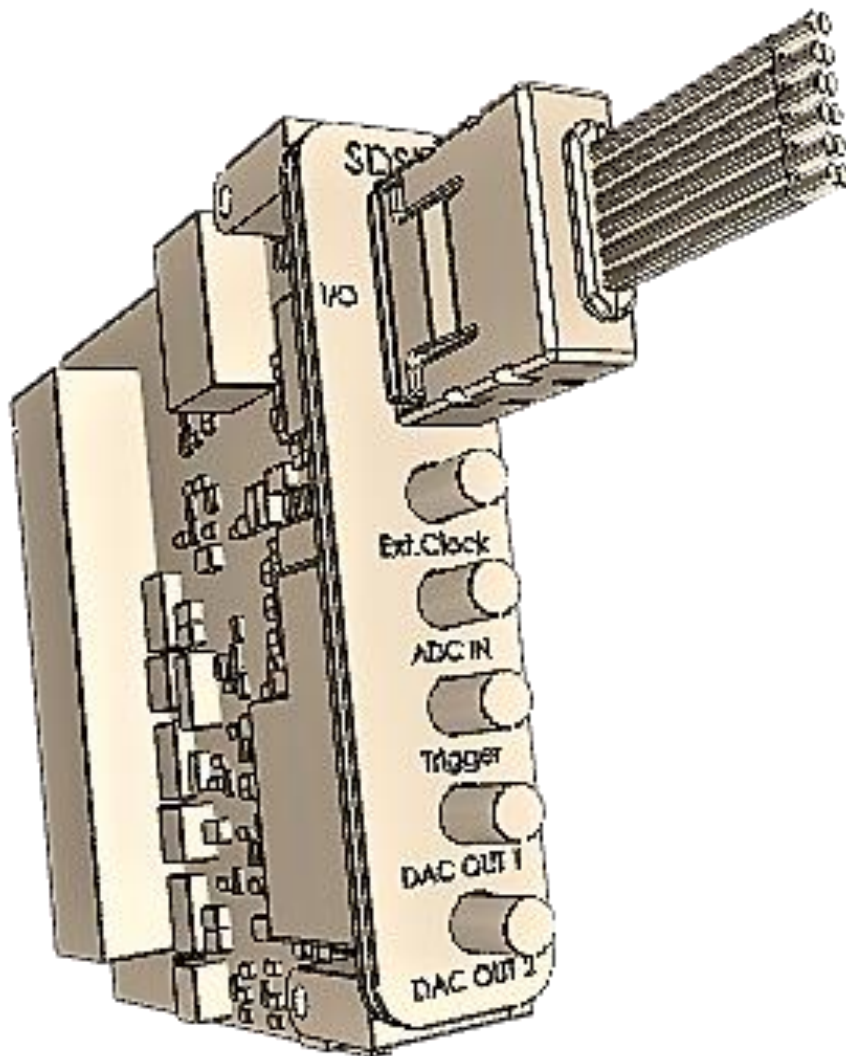| N	Row A	Row B	Row C	Row D	Row E	Row F	Row G	Row H	Row J	Row K
1	GND	GND (CLK_DIR)	GND	PG_C2M (I)	GND	PG_M2C(O)	GND	NC	GND	NC
2	ADC_DOUT1+ (FMC_M2C_DP1+)	GND	DAC_DIN0+ (FMC_C2M_DP0+)	GND	NC	GND	P/D 22R (M2C_CLK1+)	GND (FMC_PRSNT_M2C)	P/D 22R (CLK3_BDIR_P)	GND
3	ADC_DOUT1- (FMC_M2C_DP1-)	GND	DAC_DIN0- (FMC_C2M_DP0-)	GND	NC	GND	P/U 22R to VADJ (M2C_CLK1-)	GND	P/U 22R to VADJ (CLK3_BDIR_N)	GND
4	GND	To Molex CN FMC_M2C_DP9+	GND	FMC_GBTCLK0+	GND	NC	GND	FPGA_TXCLK+ (FMC_M2C_CLK0+)	GND	P/D 22R (CLK2_BDIR_P)
5	GND	To Molex CN FMC_M2C_DP9-	GND	FMC_GBTCLK0-	GND	NC	GND	FPGA_TXCLK- (FMC_M2C_CLK0-)	GND	P/U 22R to VADJ (CLK2_BDIR_N)
6	ADC_DOUT2+ (FMC_M2C_DP2+)	GND	ADC_DOUT0+ (FMC_M2C_DP0+)	GND	NC	GND	FPGA_RXCLK+(O) (FMC_CC_LA00+)	GND	NC	GND
7	ADC_DOUT2- (FMC_M2C_DP2-)	GND	ADC_DOUT0- (FMC_M2C_DP0-)	GND	NC	NC	FPGA_RXCLK-(O) (FMC_CC_LA00-)	FPGA_RXSYSREF+ (FMC_LA02+)(O)	NC	NC
8	GND	To Molex CN FMC_M2C_DP8+	GND	SPI_SDO (O) (FMC_CC_LA01+)	GND	NC	GND	FPGA_RXSYSREF- (FMC_LA02-)(O)	GND	NC
9	GND	To Molex CN FMC_M2C_DP8-	GND	SPI_ADC_CS# (I) (FMC_CC_LA01-)	NC	GND	SPI_CLK (I) (FMC_LA03+)	GND	NC	GND
10	ADC_DOUT3+ (FMC_M2C_DP3+)	GND	FPGA_TXSYSREF+ (FMC_LA06+)(O)	GND	NC	NC	SPI_SDI (I) (FMC_LA03-)	DAC_SYNCOUT1+ (FMC_LA04+)(O)	NC	NC
11	ADC_DOUT3- (FMC_M2C_DP3-)	GND	FPGA_TXSYSREF- (FMC_LA06-)(O)	ADC_TMST+ (I) (FMC_LA05+)	GND	NC	GND	DAC_SYNCOUT1- (FMC_LA04-)(O)	GND	NC
12	GND	ADC_DOUT7+ (FMC_M2C_DP7+)	GND	ADC_TMST- (I) (FMC_LA05-)	NC	GND	CLK_SDIO (O/I) (FMC_LA08+)	GND	NC	GND
13	GND	ADC_DOUT7- (FMC_M2C_DP7-)	GND	GND	NC	NC	CLK_SCLK (I) (FMC_LA08-)	DAC_SYNCOUT0+ (FMC_LA07+)(O)	NC	NC
14	ADC_DOUT4+ (FMC_M2C_DP4+)	GND	ADC_SYNC# (I) (FMC_LA10+)	CLK_CS# (I) (FMC_LA09+)	GND	NC	GND	DAC_SYNCOUT0- (FMC_LA07-)(O)	GND	NC
15	ADC_DOUT4- (FMC_M2C_DP4-)	GND	TRIGGER (O) (FMC_LA10-)	SPI_DAC_CS# (FMC_LA09-)(I)	NC	GND	ADC_OVRR0 (O) (FMC_LA12+)	GND	NC	GND
16	GND	ADC_DOUT6+ (FMC_M2C_DP6+)	GND	GND	NC	NC	ADC_OVRR1 (O) (FMC_LA12-)	ADC_TEMPCRIT# (FMC_LA11+)(O)	NC	NC
17	GND	ADC_DOUT6- (FMC_M2C_DP6-)	GND	DAC_TXEN0 (I) (FMC_LA13+)	GND	NC	GND	CLK_GPIO# (FMC_LA11-)(O)	GND	NC
18	ADC_DOUT5+ (FMC_M2C_DP5+)	GND	DAC_IRQ# (O) (FMC_LA14+)	DAC_TXEN1 (I) (FMC_LA13-)	NC	GND	To Molex CN FMC_LA16+	GND	NC	GND
19	ADC_DOUT5- (FMC_M2C_DP5-)	GND	To Molex CN (FMC_LA14-)	GND	NC	NC	To Molex CN FMC_LA16-	To Molex CN FMC_LA15+	NC	NC

N	Row A	Row B	Row C	Row D	Row E	Row F	Row G	Row H	Row J	Row K
20	GND	NC	GND	NC	GND	NC	GND	To Molex CN FMC_LA15+	GND	NC
21	GND	NC	GND	NC	NC	GND	NC	GND	NC	GND
22	DAC_DIN1+ (FMC_C2M_DP1+)	GND	NC	GND	NC	NC	NC	NC	NC	NC
23	DAC_DIN1+ (FMC_C2M_DP1-)	GND	NC	NC	GND	NC	GND	NC	GND	NC
24	GND	To Molex CN FMC_C2M_DP9+	GND	NC	NC	GND	NC	GND	NC	GND
25	GND	To Molex CN FMC_C2M_DP9-	GND	GND	NC	NC	NC	NC	NC	NC
26	DAC_DIN2+ (FMC_C2M_DP2+)	GND	NC	NC	GND	NC	GND	NC	GND	NC
27	DAC_DIN2- (FMC_C2M_DP2-)	GND	NC	NC	NC	GND	NC	GND	NC	GND
28	GND	To Molex CN FMC_C2M_DP8+	GND	GND	NC	NC	NC	NC	NC	NC
29	GND	To Molex CN FMC_C2M_DP8-	GND	NC	GND	NC	GND	NC	GND	NC
30	DAC_DIN3+ (FMC_C2M_DP3+)	GND	FMC_SCL	Pins are shorted together (FMC_TDI) (FMC_TDO)	NC	GND	NC	GND	NC	GND
31	DAC_DIN3- (FMC_C2M_DP3-)	GND	FMC_SDA		NC	NC	NC	NC	NC	NC
32	GND	DAC_DIN7+ (FMC_C2M_DP7+)	GND	To EEPROM V3P3_AUX	GND	NC	GND	NC	GND	NC
33	GND	DAC_DIN7- (FMC_C2M_DP7-)	GND	NC	NC	GND	NC	GND	NC	GND
34	DAC_DIN4+ (FMC_C2M_DP4+)	GND	To A0 of EEPROM (FMC_GA0)	NC	NC	NC	NC	NC	NC	NC
35	DAC_DIN4- (FMC_C2M_DP4-)	GND	V12P0	To A1 of EEPROM (FMC_GA1)	GND	NC	GND	NC	GND	NC
36	GND	DAC_DIN6+ (FMC_C2M_DP6+)	GND	V3P3	NC	GND	NC	GND	NC	GND
37	GND	DAC_DIN6- (FMC_C2M_DP6-)	V12P0	GND	NC	NC	NC	NC	NC	NC
38	DAC_DIN5+ (FMC_C2M_DP5+)	GND	GND	V3P3	GND	NC	GND	NC	GND	NC
39	DAC_DIN5- (FMC_C2M_DP5-)	GND	V3P3	GND	VADJ	GND	VADJ	GND	NC	GND
40	GND	NC	GND	V3P3	GND	VADJ	GND	VADJ	GND	NC

*Notes: Names in bracket – signal names according to Vita57.1.

　(O) – output from FMC_DAQ2p5, (i) – input to FMC_DAQ2p5; p/u 22R to VADJ – pull-up resistor to VADJ rail on this pin;   p/d 22R– pull-down resistor to GND on this pin;   To Molex CN – signals directly goes to Molex Nano pitch connector.

5.2 FMC pinout row wise

ROW A		
Signal Name	FMC Pin	FMC Signal
ADC_DOUT1+	A2	FMC_M2C_DP1+
ADC_DOUT1-	A3	FMC_M2C_DP1-
ADC_DOUT2+	A6	FMC_M2C_DP2+
ADC_DOUT2-	A7	FMC_M2C_DP2-
ADC_DOUT3+	A10	FMC_M2C_DP3+
ADC_DOUT3-	A11	FMC_M2C_DP3-
ADC_DOUT4+	A14	FMC_M2C_DP4+
ADC_DOUT4-	A15	FMC_M2C_DP4-
ADC_DOUT5+	A18	FMC_M2C_DP5+
ADC_DOUT5-	A19	FMC_M2C_DP5-
DAC_DIN1+	A22	FMC_C2M_DP1+
DAC_DIN1-	A23	FMC_C2M_DP1-
DAC_DIN2+	A26	FMC_C2M_DP2+
DAC_DIN2-	A27	FMC_C2M_DP2-
DAC_DIN3+	A30	FMC_C2M_DP3+
DAC_DIN3-	A31	FMC_C2M_DP3-
DAC_DIN4+	A34	FMC_C2M_DP4+
DAC_DIN4-	A35	FMC_C2M_DP4-
DAC_DIN5+	A38	FMC_C2M_DP5+
DAC_DIN5-	A39	FMC_C2M_DP5-

ROW B		
Signal Name	FMC Pin	FMC Signal
MOLEX_RX1+	B4	FMC_M2C_DP9+
MOLEX_RX1-	B5	FMC_M2C_DP9-
MOLEX_RX0+	B8	FMC_M2C_DP8+
MOLEX_RX0-	B9	FMC_M2C_DP8-
ADC_DOUT7+	B12	FMC_M2C_DP7+
ADC_DOUT7-	B13	FMC_M2C_DP7-
ADC_DOUT6+	B16	FMC_M2C_DP6+
ADC_DOUT6-	B17	FMC_M2C_DP6-
MOLEX_TX1+	B24	FMC_C2M_DP9+
MOLEX_TX1-	B25	FMC_C2M_DP9-
MOLEX_TX1+	B28	FMC_C2M_DP8+
MOLEX_TX1-	B29	FMC_C2M_DP8-
DAC_DIN7+	B32	FMC_C2M_DP7+
DAC_DIN7-	B33	FMC_C2M_DP7-
DAC_DIN6+	B36	FMC_C2M_DP6+
DAC_DIN6-	B37	FMC_C2M_DP6-

ROW C		
Signal Name	FMC Pin	FMC Signal
DAC_DIN0+	C2	FMC_C2M_DP0+
DAC_DIN0-	C3	FMC_C2M_DP0-
ADC_DOUT0+	C6	FMC_M2C_DP0+
ADC_DOUT0-	C7	FMC_M2C_DP0-
FPGA_TXSYSREF+	C10	FMC_LA06+
FPGA_TXSYSREF-	C11	FMC_LA06-
ADC_SYNC	C14	FMC_LA10+

TRIGGER	C15	FMC_LA10-
DAC_IRQ	C18	FMC_LA14+
MOLEX_GPIO1	C19	FMC_LA14-
MOLEX_SCL	C30	FMC_SCL
MOLEX_SDA	C31	FMC_SDA

ROW D		
Signal Name	**FMC Pin**	**FMC Signal**
HMC7044_CLK4+	D4	FMC_GBTCLK0+
HMC7044_CLK4-	D5	FMC_GBTCLK0-
DAQ_SPI_SDO	D8	FMC_CC_LA01+
ADC_SPI_CS#	D9	FMC_CC_LA01-
ADC_TMST+	D11	FMC_LA05+
ADC_TMST-	D12	FMC_LA05-
CLK_SPI_CS#	D14	FMC_LA09+
DAC_SPI_CS#	D15	FMC_LA09-
DAC_TXEN0	D17	FMC_LA13+
DAC_TXEN1	D18	FMC_LA13-

ROW G		
Signal Name	**FMC Pin**	**FMC Signal**
FPGA_RXCLK+	G6	FMC_CC_LA00+
FPGA_RXCLK-	G7	FMC_CC_LA00-
DAQ_SPI_SCLK	G9	FMC_LA03+
DAQ_SPI_SDI	G10	FMC_LA03-
CLK_SPI_SDIO	G12	FMC_LA08+
CLK_SPI_SCLK	G13	FMC_LA08-
ADC_OVRR0	G15	FMC_LA12+
ADC_OVRR1	G16	FMC_LA12-
MOLEX_DP1+	G18	FMC_LA16+

MOLEX_DP1-	G19	FMC_LA16-

ROW H		
Signal Name	FMC Pin	FMC Signal
FPGA_TXCLK+	H4	FMC_M2C_CLK0+
FPGA_TXCLK-	H5	FMC_M2C_CLK0-
FPGA_RXSYSREF+	H7	FMC_LA02+
FPGA_RXSYSREF-	H8	FMC_LA02-
DAC_SYNCOUT1+	H10	FMC_LA04+
DAC_SYNCOUT1-	H11	FMC_LA04-
DAC_SYNCOUT0+	H13	FMC_LA07+
DAC_SYNCOUT0-	H14	FMC_LA07-
ADC_TEMP_CTRL	H16	FMC_LA11+
CLK_GPIO	H17	FMC_LA11-
MOLEX_DP0+	H19	FMC_LA15+
MOLEX_DP0-	H20	FMC_LA15-

5.3 Pinout for Molex nano pitch 171982-0142 connector

Molex pin No	Signal name	Comment	Molex pin No	Signal NAME	Comment
A1	-	Not connected	B1	-	Not connected
A2	GND	Ground	B2	GND	Ground
A3	MOLEX_RX0+	AC coupled, 16 Gb/s, Dir. From Molex to HPC Connector	B3	MOLEX_TX0+	AC coupled, 16 Gb/s, Dir. From HPC to Molex Connector. Request 100 Ohm diff. termination.
A4	MOLEX_RX0-		B4	MOLEX_TX0-	
A5	GND	Ground	B5	GND	Ground
A6	MOLEX_RX1+	AC coupled, 16 Gb/s, Dir. From Molex to	B6	MOLEX_TX1+	AC coupled, 16 Gb/s, Dir. From HPC to Molex

A7	MOLEX_RX1-	HPC Connector.	B7	MOLEX_TX1-	Connector. Request 100 Ohm diff. termination.
A8	GND	Ground	B8	GND	Ground
A9	MOLEX_SDA	3.3V level. Also connected to EEPROM 24C16	B9	GND	Ground
A10	MOLEX_SCL		B10	-	Not connected
A11	GND	Ground	B11	GND	Ground
A12	VCC_ADJ_FMC	Direct connection to VADJ.	B12	GND	Ground
A13		May be 1.8V or 2.5V or 3.3V. Used as reference for I/Os	B13	MOLEX_GPIO1	I/O, DC coupled. Max V is VADJ.
A14	GND	Ground	B14	GND	Ground
A15	MOLEX_DP0+	I/Os, DC coupled. Max V is VADJ.	B15	MOLEX_SYSREF+	Clock output, or JESD204B SYSREF output. AC coupled. Fmax = 3.2GHz
A16	MOLEX_DP0-		B16	MOLEX_SYSREF-	
A17	GND	Ground	B17	GND	Ground
A18	MOLEX_DP1+	I/Os, DC coupled. Max V is VADJ.	B18	MOLEX_CLK+	Clock output. AC coupled. Fmax = 3.2GHz
A19	MOLEX_DP1-		B19	MOLEX_CLK-	
A20	GND	Ground	B20	GND	Ground

6 REFERENCE LIST

A set of links for your easy access to guides for devices used on this module:

AD9136 – 16 bit 2.8GSPS Dual channel DAC;
ADC12J2700 – 12 bit single channel 2.7 GSPS ADC;
HMC7044 – High performance 3.2GHz JESD204B clock jitter cleaner;
PG066-JESD204.pdf – JESD204B Logic core IP user guide.
ADC12J2700 GUI – GUI for ADC configuration.
DAC software suite – GUI for DAC configuration.
HMC704x software – GUI for HMC7044 clock IC configuration.

7 COOLING

User must make sure that adequate air flow and cooling is provided for using this module.

8 SAFETY

The module presents no hazard to the user.

9 EMC

The module is designed to operate within an enclosed host system that provides adequate EMC shielding.
Operation within the EU EMC guidelines is only guaranteed when the module is installed within an appropriate host system.
The module is protected from damage by fast voltage transients introduced along output cables from outside the host system.
Short-circuiting any output to ground does not cause the host PC system to lock up or reboot.

10 ORDERING INFORMATION

FMC-DAQ2p5   This is the default model with 1 ADC channel and 2 DAC channel

FMC-2p5-ADC**0**-DAC**2**   0x ADC and 2x DAC channels,

FMC-2p5-ADC**1**-DAC**0**   1x ADC and 0x DAC channels,