

Creative uses of FMC

Introduction by
Jerry Gipper



The FPGA Mezzanine Card (FMC) standard has become the defacto mezzanine standard for anyone wanting a modular solution for platforms using an FPGA [field-programmable gate array]. The convenience of having modular I/O for any FPGA family makes it hard to not use an FMC as the I/O front-end. Consequently, the FMC standard, VITA 57, has gained worldwide acceptance and is endorsed by the major FPGA manufacturers.

The FMC technical community has been working diligently on upgrades for what is known as FMC+, calling for a new set of connectors to support higher-speed serial interfaces. FMC+ augments the FMC interface by adding 14 additional full duplex high speed serial lanes for 24 total. Beyond FMC+, VITA 57.4 also has a provision for even more high-speed serial lanes. FMC+e calls for a mechanically separate connector to the primary FMC+ connector, adding eight more high-speed serial lanes, bringing the total possible to 32.

The engineering community has been getting creative in ways to leverage the modularity of FMC. Let's take a look at some of those applications.

Optimizing pin utilization with FMC stacking

By *Abaco Systems*

Advances in I/O technology have led to multiple signal types being defined for the FMC interface. Additionally, FPGA density and complexity has led to higher device cost, making I/O pins a valuable commodity in any FPGA-based system. Rapid advancement in both FPGA and ADC/DAC technology has led designers to favor modular solutions to accommodate future upgrades without requiring a complete system re-architecture.

The FMC connector is a 400-pin interface accommodating both low-voltage differential signaling (LVDS) and high-speed serial pins as shown in Figure 1. It should be noted that the term 'serial lane' often refers to a bundle of two differential pairs: a mezzanine-to-carrier (M2C) differential pair and a carrier-to-mezzanine (C2M) differential pair. This distinction is critical to understand the FMC stacking technology. It is important to note that I/O and clocks dedicated to serial lanes often require connection to specialized pins on the FPGA. Thus, engineers must take care when designing both carrier and FMC to ensure these pins are mapped appropriately.

FMC interfaces are designed to accommodate both LVDS and high-speed serial interfaces. Often, FMC designs don't require using all I/O, leaving valuable FPGA pins unused and wasted. If intentionally designed in, these unused pins can be utilized by passing these wires to the topside of the board in an intelligent way to enable FMC stacking.

An example of a board with this capability is the Abaco Systems FMC216 shown in Figure 2. This design includes 16 analog output channels at 312.5 MSPS at 16-bits. The FMC216 requires eight high-speed serial lanes from the carrier-to-mezzanine (C2M) and four of the LVDS lanes. This leaves the FMC216 with 10 M2C lanes, 2 C2M lanes, and 76 LVDS lanes unused.

VITA 57.1 calls for all LVDS and serial lanes to be populated in ascending order; thus, the FMC216 re-maps unused pins from the bottom of the board to the top of the board starting at index zero on its respective bus. The topside FMC interface now only has 76 LVDS I/O, all 10 M2C lanes, and only 2 C2M lanes – making it a partially compliant FMC site. If a subsequent FMC board only requires a subset of the LVDS or high-speed serial lanes, an additional FMC can be stacked. The Abaco Systems FMC116 is designed to specifically pair with the FMC216 to create a compact MIMO solution with 16 DACs and 16 ADCs. This matched pair can then be placed on any compliant carrier board.

Limitation and practical considerations
 FMC stacking is a way to utilize more of the valuable resources on the FMC interface and connect more sensing capabilities to a single FPGA card, thus reducing the overall system cost. However, it does require the pair of FMCs to be analyzed carefully to ensure compatibility. FMC stacking is a natural consequence of the evolution of I/O types and the FMC standard accommodating both LVDS and high-speed serial. When utilizing FMC stacking, engineers must account for the additional spacing required – often calling for an additional slot in PCIe or VPX systems. Special cooling considerations may be required depending on the FMC type.

FPGA and I/O technologies have shown significant evolution over the past 25 years, from very simple devices to systems-on-chip (SoC) with 1000s of pins. System integrators are more often looking to build systems on modular components based on standard interface.

K	J	H	G	F	E	D	C	B	A
VREF_B_M2C	GND	REF_A_M2C	GND	PG_M2C	GND	High Speed Serial (One Lane)		CLK_DR	GND
GND	DIR_P	RSMT_M2C	M2C_P	GND	HA01_P_CC	LA01_P	LA01_N	GND	DP1_M2C
GND	DIR_N	GND	M2C_N	GND	HA01_N_CC	LA01_N	LA01_P	GND	DP1_M2C
CLK_B_M2C	GND	SLD0_M2C	GND	HA03_P_CC	GND	LA03_P	LA03_N	GND	DP5_M2C_P
CLK_B_M2C	GND	SLD0_M2C	GND	HA03_N_CC	GND	LA03_N	LA03_P	GND	DP5_M2C_N
GND	HA03_P	GND	LA03_P	HA05_P	GND	LA05_P	LA05_N	GND	DP5_M2C
HA03_N	GND	LA03_N	LA03_N	HA05_N	GND	LA05_N	LA05_P	GND	DP5_M2C
GND	HA07_P	GND	LA07_P	HA09_P	GND	LA09_P	LA09_N	GND	DP5_M2C
HA07_N	GND	LA07_N	LA07_N	HA09_N	GND	LA09_N	LA09_P	GND	DP5_M2C
GND	HA11_P	GND	LA11_P	HA13_P	GND	LA13_P	LA13_N	GND	DP5_M2C
HA11_N	GND	LA11_N	LA11_N	HA13_N	GND	LA13_N	LA13_P	GND	DP5_M2C
GND	HA15_P	GND	LA15_P	HA17_P	GND	LA17_P	LA17_N	GND	DP5_M2C
HA15_N	GND	LA15_N	LA15_N	HA17_N	GND	LA17_N	LA17_P	GND	DP5_M2C
HA17_P_CC	HA14_P	GND	LA17_P	HA19_P	GND	LA19_P	LA19_N	GND	DP5_M2C
HA17_N_CC	HA14_N	GND	LA17_N	HA19_N	GND	LA19_N	LA19_P	GND	DP5_M2C
GND	HA18_P	GND	LA18_P	HA21_P	GND	LA21_P	LA21_N	GND	DP5_M2C
HA18_N	GND	LA18_N	LA18_N	HA21_N	GND	LA21_N	LA21_P	GND	DP5_M2C
GND	HA22_P	GND	LA22_P	HA24_P	GND	LA24_P	LA24_N	GND	DP5_M2C
HA22_N	GND	LA22_N	LA22_N	HA24_N	GND	LA24_N	LA24_P	GND	DP5_M2C
GND	HA26_P	GND	LA26_P	HA28_P	GND	LA28_P	LA28_N	GND	DP5_M2C
HA26_N	GND	LA26_N	LA26_N	HA28_N	GND	LA28_N	LA28_P	GND	DP5_M2C
GND	HA30_P	GND	LA30_P	HA32_P	GND	LA32_P	LA32_N	GND	DP5_M2C
HA30_N	GND	LA30_N	LA30_N	HA32_N	GND	LA32_N	LA32_P	GND	DP5_M2C
GND	HA34_P	GND	LA34_P	HA36_P	GND	LA36_P	LA36_N	GND	DP5_M2C
HA34_N	GND	LA34_N	LA34_N	HA36_N	GND	LA36_N	LA36_P	GND	DP5_M2C
GND	HA38_P	GND	LA38_P	HA40_P	GND	LA40_P	LA40_N	GND	DP5_M2C
HA38_N	GND	LA38_N	LA38_N	HA40_N	GND	LA40_N	LA40_P	GND	DP5_M2C
GND	HA42_P	GND	LA42_P	HA44_P	GND	LA44_P	LA44_N	GND	DP5_M2C
HA42_N	GND	LA42_N	LA42_N	HA44_N	GND	LA44_N	LA44_P	GND	DP5_M2C
GND	HA46_P	GND	LA46_P	HA48_P	GND	LA48_P	LA48_N	GND	DP5_M2C
HA46_N	GND	LA46_N	LA46_N	HA48_N	GND	LA48_N	LA48_P	GND	DP5_M2C
GND	HA50_P	GND	LA50_P	HA52_P	GND	LA52_P	LA52_N	GND	DP5_M2C
HA50_N	GND	LA50_N	LA50_N	HA52_N	GND	LA52_N	LA52_P	GND	DP5_M2C
GND	HA54_P	GND	LA54_P	HA56_P	GND	LA56_P	LA56_N	GND	DP5_M2C
HA54_N	GND	LA54_N	LA54_N	HA56_N	GND	LA56_N	LA56_P	GND	DP5_M2C
GND	HA60_P	GND	LA60_P	HA62_P	GND	LA62_P	LA62_N	GND	DP5_M2C
HA60_N	GND	LA60_N	LA60_N	HA62_N	GND	LA62_N	LA62_P	GND	DP5_M2C
GND	HA64_P	GND	LA64_P	HA66_P	GND	LA66_P	LA66_N	GND	DP5_M2C
HA64_N	GND	LA64_N	LA64_N	HA66_N	GND	LA66_N	LA66_P	GND	DP5_M2C
GND	HA70_P	GND	LA70_P	HA72_P	GND	LA72_P	LA72_N	GND	DP5_M2C
HA70_N	GND	LA70_N	LA70_N	HA72_N	GND	LA72_N	LA72_P	GND	DP5_M2C
GND	HA74_P	GND	LA74_P	HA76_P	GND	LA76_P	LA76_N	GND	DP5_M2C
HA74_N	GND	LA74_N	LA74_N	HA76_N	GND	LA76_N	LA76_P	GND	DP5_M2C
GND	HA80_P	GND	LA80_P	HA82_P	GND	LA82_P	LA82_N	GND	DP5_M2C
HA80_N	GND	LA80_N	LA80_N	HA82_N	GND	LA82_N	LA82_P	GND	DP5_M2C
GND	HA84_P	GND	LA84_P	HA86_P	GND	LA86_P	LA86_N	GND	DP5_M2C
HA84_N	GND	LA84_N	LA84_N	HA86_N	GND	LA86_N	LA86_P	GND	DP5_M2C
GND	HA90_P	GND	LA90_P	HA92_P	GND	LA92_P	LA92_N	GND	DP5_M2C
HA90_N	GND	LA90_N	LA90_N	HA92_N	GND	LA92_N	LA92_P	GND	DP5_M2C
GND	HA94_P	GND	LA94_P	HA96_P	GND	LA96_P	LA96_N	GND	DP5_M2C
HA94_N	GND	LA94_N	LA94_N	HA96_N	GND	LA96_N	LA96_P	GND	DP5_M2C
GND	HA100_P	GND	LA100_P	HA102_P	GND	LA102_P	LA102_N	GND	DP5_M2C
HA100_N	GND	LA100_N	LA100_N	HA102_N	GND	LA102_N	LA102_P	GND	DP5_M2C
GND	HA104_P	GND	LA104_P	HA106_P	GND	LA106_P	LA106_N	GND	DP5_M2C
HA104_N	GND	LA104_N	LA104_N	HA106_N	GND	LA106_N	LA106_P	GND	DP5_M2C
GND	HA110_P	GND	LA110_P	HA112_P	GND	LA112_P	LA112_N	GND	DP5_M2C
HA110_N	GND	LA110_N	LA110_N	HA112_N	GND	LA112_N	LA112_P	GND	DP5_M2C
GND	HA114_P	GND	LA114_P	HA116_P	GND	LA116_P	LA116_N	GND	DP5_M2C
HA114_N	GND	LA114_N	LA114_N	HA116_N	GND	LA116_N	LA116_P	GND	DP5_M2C
GND	HA120_P	GND	LA120_P	HA122_P	GND	LA122_P	LA122_N	GND	DP5_M2C
HA120_N	GND	LA120_N	LA120_N	HA122_N	GND	LA122_N	LA122_P	GND	DP5_M2C
GND	HA124_P	GND	LA124_P	HA126_P	GND	LA126_P	LA126_N	GND	DP5_M2C
HA124_N	GND	LA124_N	LA124_N	HA126_N	GND	LA126_N	LA126_P	GND	DP5_M2C
GND	HA130_P	GND	LA130_P	HA132_P	GND	LA132_P	LA132_N	GND	DP5_M2C
HA130_N	GND	LA130_N	LA130_N	HA132_N	GND	LA132_N	LA132_P	GND	DP5_M2C
GND	HA134_P	GND	LA134_P	HA136_P	GND	LA136_P	LA136_N	GND	DP5_M2C
HA134_N	GND	LA134_N	LA134_N	HA136_N	GND	LA136_N	LA136_P	GND	DP5_M2C
GND	HA140_P	GND	LA140_P	HA142_P	GND	LA142_P	LA142_N	GND	DP5_M2C
HA140_N	GND	LA140_N	LA140_N	HA142_N	GND	LA142_N	LA142_P	GND	DP5_M2C
GND	HA144_P	GND	LA144_P	HA146_P	GND	LA146_P	LA146_N	GND	DP5_M2C
HA144_N	GND	LA144_N	LA144_N	HA146_N	GND	LA146_N	LA146_P	GND	DP5_M2C
GND	HA150_P	GND	LA150_P	HA152_P	GND	LA152_P	LA152_N	GND	DP5_M2C
HA150_N	GND	LA150_N	LA150_N	HA152_N	GND	LA152_N	LA152_P	GND	DP5_M2C
GND	HA154_P	GND	LA154_P	HA156_P	GND	LA156_P	LA156_N	GND	DP5_M2C
HA154_N	GND	LA154_N	LA154_N	HA156_N	GND	LA156_N	LA156_P	GND	DP5_M2C
GND	HA160_P	GND	LA160_P	HA162_P	GND	LA162_P	LA162_N	GND	DP5_M2C
HA160_N	GND	LA160_N	LA160_N	HA162_N	GND	LA162_N	LA162_P	GND	DP5_M2C
GND	HA164_P	GND	LA164_P	HA166_P	GND	LA166_P	LA166_N	GND	DP5_M2C
HA164_N	GND	LA164_N	LA164_N	HA166_N	GND	LA166_N	LA166_P	GND	DP5_M2C
GND	HA170_P	GND	LA170_P	HA172_P	GND	LA172_P	LA172_N	GND	DP5_M2C
HA170_N	GND	LA170_N	LA170_N	HA172_N	GND	LA172_N	LA172_P	GND	DP5_M2C
GND	HA174_P	GND	LA174_P	HA176_P	GND	LA176_P	LA176_N	GND	DP5_M2C
HA174_N	GND	LA174_N	LA174_N	HA176_N	GND	LA176_N	LA176_P	GND	DP5_M2C
GND	HA180_P	GND	LA180_P	HA182_P	GND	LA182_P	LA182_N	GND	DP5_M2C
HA180_N	GND	LA180_N	LA180_N	HA182_N	GND	LA182_N	LA182_P	GND	DP5_M2C
GND	HA184_P	GND	LA184_P	HA186_P	GND	LA186_P	LA186_N	GND	DP5_M2C
HA184_N	GND	LA184_N	LA184_N	HA186_N	GND	LA186_N	LA186_P	GND	DP5_M2C
GND	HA190_P	GND	LA190_P	HA192_P	GND	LA192_P	LA192_N	GND	DP5_M2C
HA190_N	GND	LA190_N	LA190_N	HA192_N	GND	LA192_N	LA192_P	GND	DP5_M2C
GND	HA194_P	GND	LA194_P	HA196_P	GND	LA196_P	LA196_N	GND	DP5_M2C
HA194_N	GND	LA194_N	LA194_N	HA196_N	GND	LA196_N	LA196_P	GND	DP5_M2C
GND	HA200_P	GND	LA200_P	HA202_P	GND	LA202_P	LA202_N	GND	DP5_M2C
HA200_N	GND	LA200_N	LA200_N	HA202_N	GND	LA202_N	LA202_P	GND	DP5_M2C
GND	HA204_P	GND	LA204_P	HA206_P	GND	LA206_P	LA206_N	GND	DP5_M2C
HA204_N	GND	LA204_N	LA204_N	HA206_N	GND	LA206_N	LA206_P	GND	DP5_M2C
GND	HA210_P	GND	LA210_P	HA212_P	GND	LA212_P	LA212_N	GND	DP5_M2C
HA210_N	GND	LA210_N	LA210_N	HA212_N	GND	LA212_N	LA212_P	GND	DP5_M2C
GND	HA214_P	GND	LA214_P	HA216_P	GND	LA216_P	LA216_N	GND	DP5_M2C
HA214_N	GND	LA214_N	LA214_N	HA216_N	GND	LA216_N	LA216_P	GND	DP5_M2C
GND	HA220_P	GND	LA220_P	HA222_P	GND	LA222_P	LA222_N	GND	DP5_M2C
HA220_N	GND	LA220_N	LA220_N	HA222_N	GND	LA222_N	LA222_P	GND	DP5_M2C
GND	HA224_P	GND	LA224_P	HA226_P	GND	LA226_P	LA226_N	GND	DP5_M2C
HA224_N	GND	LA224_N	LA224_N	HA226_N	GND	LA226_N	LA226_P	GND	DP5_M2C
GND	HA230_P	GND	LA230_P	HA232_P	GND	LA232_P	LA232_N	GND	DP5_M2C
HA230_N	GND	LA230_N	LA230_N	HA232_N	GND	LA232_N	LA232_P	GND	DP5_M2C
GND	HA234_P	GND	LA234_P	HA236_P	GND	LA236_P	LA236_N	GND	DP5_M2C
HA234_N	GND	LA234_N	LA234_N	HA236_N	GND	LA236_N	LA236_P	GND	DP5_M2C
GND	HA240_P	GND	LA240_P	HA242_P	GND	LA242_P	LA242_N	GND	DP5_M2C
HA240_N	GND	LA240_N	LA240_N	HA242_N	GND	LA242_N	LA242_P	GND	DP5_M2C
GND	HA244_P	GND	LA244_P	HA246_P	GND	LA246_P	LA246_N	GND	DP5_M2C
HA244_N	GND	LA244_N	LA244_N	HA246_N	GND	LA246_N	LA246_P	GND	DP5_M2C
GND	HA250_P	GND	LA250_P	HA252_P	GND	LA252_P	LA252_N	GND	DP5_M2C
HA250_N	GND	LA250_N	LA250_N	HA252_N	GND	LA252_N	LA252_P	GND	DP5_M2C
GND	HA254_P	GND	LA254_P	HA256_P	GND	LA256_P	LA256_N	GND	DP5_M2C
HA254_N	GND	LA254_N	LA254_N	HA256_N	GND	LA256_N	LA256_P	GND	DP5_M2C
GND	HA260_P	GND	LA260						

VITA defined the FPGA mezzanine card to accommodate both parallel and serial I/O pin classes: however, many FMC board designs don't use all available resource pins, leaving extremely valuable FPGA I/O unused. FMC stacking is a technique to get back unused pins on an FMC interface. The CES821 with the FMC216 and FMC116 was given as an example of an integrated solution implementing this technique to not only use as many of the valuable FPGA pins as possible, but also do so in an extremely compact embedded system. When considering I/O system requirements in an FPGA-based system, it is possible to leverage Abaco FMC Stacking technology to ensure valuable FPGA pins do not sit idle.

PXI, meet FMC

By Sundance Multiprocessor Technology

PXI and FMC have different roots and have historically served differing markets. So separate are the markets, that most users are familiar with either one or the other, but not both. However, creatively combining the two standards onto a single product can expand the advantages of either past their current application space.

PXI is a modular pluggable card-based standard common in test and measurement applications. It was released as a standard in 1997 as an abbreviation for PCI eXtensions for Instrumentation, and is maintained by the PXI Systems Alliance. PXI adopts the rugged CompactPCI form factor and adds integrated clocks, triggers, and synchronization critical to test and measurement applications. PXI modules fit into a multi-slot chassis, and are configured and managed by a PC and software. As PCI speeds increased by the adoption of PCIe (PCI Express), PXI has followed with high-speed PCIe fabrics in the chassis and on the modules. Though occasionally referred to as PXIe, PXI remains a generic name, whether the backplane relies on PCI or PCIe.

PXI and FMC standards can be combined into a single product by creating an FMC-compatible PXI carrier card

that allows the insertion of FMC modules. In this case, the user will end up with a fully PXI-compatible module, but with the raw measurement function defined by the FMC. Additional processing can be done by the FPGA on the carrier, on another PXI module, or by the PC software, to customize the measurement functions.

PXI AND FMC HAVE DIFFERENT ROOTS AND HAVE HISTORICALLY SERVED DIFFERING MARKETS. SO SEPARATE ARE THE MARKETS, THAT MOST USERS ARE FAMILIAR WITH EITHER ONE OR THE OTHER, BUT NOT BOTH. HOWEVER, CREATIVELY COMBINING THE TWO STANDARDS ONTO A SINGLE PRODUCT CAN EXPAND THE ADVANTAGES OF EITHER PAST THEIR CURRENT APPLICATION SPACE.

An example of this approach comes from Sundance DSP, with their PXIe700 FPGA PXIe Carrier Module. (See figure 4). The PXIe700 is a 3U PXI Express module with a FMC "site" where an arbitrary FMC module can be inserted. The mechanical positioning of the site aligns the faceplate of the FMC module with the faceplate of the PXI card, making it one integrated PXI device.

The PXIe700 carrier supports PXI control, trigger, and clocks to the backplane, including four-lane Gen 2 PCIe communications. It also supports the HPC (High Pin Count) connector to the FMC, including 10 GTX transceivers at 12.5Gb/s each, as well as 144 single ended I/Os or 72 differential I/Os.



FIGURE 4

The Sundance PXIe700 FPGA Carrier (left) without any FMC inserted. The large black connector is the electrical interface to the FMC, while the faceplate houses an opening for the FMC's front panel. The same PXI carrier (right), but with an FMC inserted, specifically the Sundance FMC-DAQ2p5. Note how the front panels align.

All of this is made possible by the onboard Xilinx Kintex7 FPGA, which connects between the PXI backplane and the FMC HPC connector. This can be seen in the Figure 5 block diagram. FMC, by its very name, is intended to interface directly with the I/O pins of an FPGA. This makes for a very high-performance low-latency interface.

Applications

The combination of a high performance PXI carrier with any of the hundreds of FMC modules allows a wide set of applications to be addressed. Though PXI was conceived as a test and measurement platform, its small rugged form factor has also allowed it to be deployed as an embedded application in industrial, medical, and military markets.

An example is using the PXIe-700 with the FMC-DAQ2P5 mezzanine to address radar applications. The FMC-DAQ2P5 hosts a 12-bit 2.7Gs/s ADC (analog-to-digital converter), two 16-bit 2.8Gs/s DACs (digital-to-analog converters), and a number of single ended and differential I/O lines. This is a good example of the high performance instrumentation that can be hosted on an FMC module. In this case, IP is downloaded into the Xilinx FPGA that both analyzes and generates the high frequency signals used in radar applications. Using Mathworks Simulink, the user can add custom algorithms. These signals may be wideband baseband signals, which can be coupled to microwave downconverters, and upconverters available in the PXI format to address the spectrum of interest. Using PXI plus FMC, a small, powerful radar system can be prototyped in a small PXI chassis.

FMC also fills an important role in PXI systems – customization. In many systems standard PXI modules need to be augmented with custom tailored instrumentation or signal conditioning. FMC allows a user to design their own custom printed circuit board that then is deployed in a PXI system via a carrier card. If more board space is needed than available on a standard FMC module, a custom design can be created that is nearly the size of a PXI module. As long

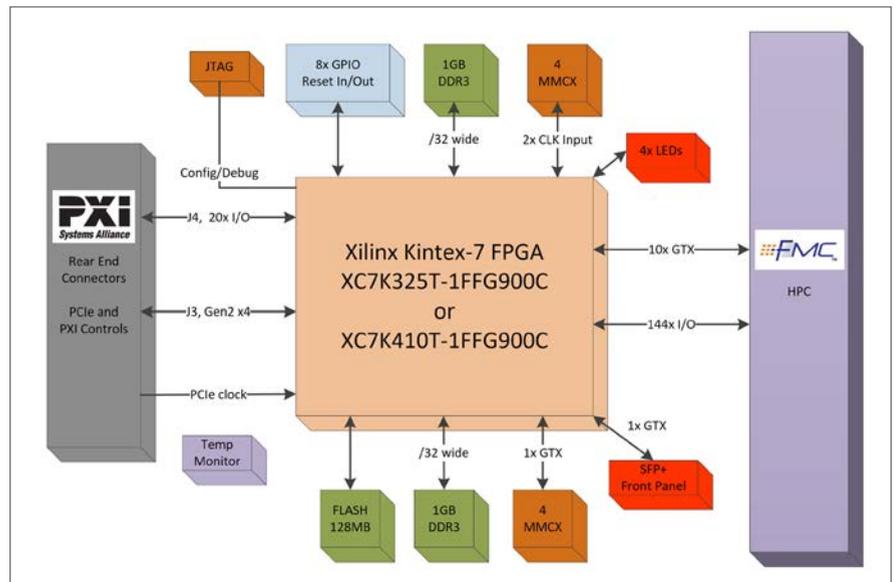


FIGURE 5

Block diagram of the PXIe-700 carrier. The embedded Xilinx FPGA contains the IP for all PXI operations to the right, as well the interfaces to the FMC on the left. The user programs the FPGA to access and control the specific FMC functions they desire.

as the custom board places the FMC HPC connector correctly, the new daughter card acts as a supersized FMC. If power dissipation is a concern, the new FMC can extend into the space of an adjacent slot, where the PXI chassis will supply ample cooling.

Sundance was not the first organization to deploy PXI plus FMC. CERN did as well, in a very sophisticated data acquisition and control system. The possible applications are only limited by the measurement functionality of FMC modules, which is growing rapidly. The combination expands PXI's addressable market from primarily test and measurement to data acquisition and control, embedded, and prototyping applications. It is also an effective method for a user to add their own custom card to a PXI system.

PXI metrology grade instrumentation coupled with the growing number of analog, digital, and RF products from FMC is a powerful combination. PXI has addressed a wide set of applications in numerous industries. Over 1500 modules are available from over 50 vendors. With PXI-based FMC carriers, the new applications are nearly endless. **VITA**

FMC BASICS

FMC is an abbreviation for FPGA Mezzanine Cards, standardized as VITA 57.1. As its name implies, FMC describes a low-profile mezzanine module envisioned to connect from above, typically onto 3U and 6U cards with the front panels aligned. It refers to these host cards as carriers, and assumes an FPGA with reprogrammable I/O exists on the carrier. The FMC modules come in two standard sizes, with a high-density 400-pin connector interfacing to the carrier card. By standardizing on the mechanical footprint and electrical interface, FMC cards can host a wide range of analog, digital, RF, and I/O functions to then be deployed onto more generic carriers, which may also span several standards.