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# EMC<sup>2</sup>-DP V2

## PCIe/104 OneBank™ Carrier for 40mm x 50mm SoM + VITA57.1 FMC™ Modules



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## Revision History

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2.0	Major update	17/9/14	GKP
2.0.1	Cosmetics	28/10/14	FC
2.0.2	Updated board layout.	5/11/14	GKP
2.0.3	Removed USB interface on PCIe104 connector. Added MIO detail. Added MEMS (accelerometer) on main board.	23/1/15	GKP
2.1.0	Added PCIe switch	6/3/15	GKP
2.2.0	Added new Visio drawings and photos	17/03/15	FC
2.2.1	Added detail to PCIe switch	1/4/15	GKP
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2.2.3	Updated photo and diagram	29/06/15	FC
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3.1	Updated title page picture (board V2 with Z7030 Trenz module)	19/02/16	TG
3.2	Updated block diagram for V2	22/02/16	TG
3.3	Updated Board parts for V2 Updated MIO Allocations for V2 Updated information RTC, USB (board)	24/02/16	TG
3.4	Removed PSU section till update	31/03/16	CH

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# 1 Introduction

This document describes the hardware features and some operational details of how the EMC<sup>2</sup>-DP will become a PCIe/104 OneBank™ Board with a Dual ARM9 CPU + Re-configurable FPGA Logic (Xilinx Zynq w. Artix-7 or Kintex-7 Fabric) and interface to CPU specific I/O features. It also covers how the EMC<sup>2</sup>-DP can be used as either a Host Controller in a PC/104 Stack or as stand-alone.

Furthermore it also covers the use of EMC<sup>2</sup>-DP with a ‘Fabric-only’ mode, with the use of either an Artix-7 or a Kintex-7 40mm x 50 mm “System-on-Module”.

Some discussion is made of how these features can be implemented with specific “System-on-Modules” and how EMC<sup>2</sup>-DP can be expanded with a VITA57.1 FMC-LPC™ compatible Daughter Cards for I/O expansion from the FPGA fabric.

## 1.1 Main Features

### 1.1.1 Hardware

This board consists of the following major hardware features:

EMC2-Z70xx: Xilinx [Zynq SoC XC7Z015](#) (Artix-7) or XC7Z7030 (Kintex-7) SoM

- 1Gbyte DDR3 memory for ARM CPU to run Linux

EMC2-7Axxx Xilinx [Artix-7 FPGA SoM](#)

- 1Gbyte DDR3 memory interfaced to Fabric of FPGA

EMC2-7Kxxx Xilinx [Kintex-7 FPGA SoM](#)

- 32Mbytes Quad-SPI Flash

#### Common Features:

- Programmable clock synthesizer and external 1PPS input.
- GEN2 PCIe on top and bottom PCIe/104 connectors.
- SATA Interface to PCIe/104 bottom connector or SEIC.
- FMC LPC connector with I/O and single high-speed serial.
- Single +5, +12, +3.3V power input.
- 100-way SEIC peripheral interface connector.

## 2 Notes

Several part numbers are described in the text, as HyperLinks. These are possible part numbers, and alternative devices may be designed in at a later date. Hyperlinks will provide access to external sites for more details

### 2.1 Abbreviations / Definitions

ADC	Analog to Digital Converter.
DDR & DDR3	Dual Data Rate. An interface mechanism where data is transferred on both rising and falling clock edges. DDR3 memory is lower power and higher performance than its predecessor, DDR2.
DRAM	Dynamic RAM.
DVI	Digital Visual Interface. When used on its own in this document it refers to the digital portion of the connector's signals.
DVI-D	Digital video data only.
DVI-I	Digital and analog (VGA) data.
EEPROM	Also called E <sup>2</sup> PROM (or just E <sup>2</sup> ). Electrically erasable and programmable ROM.
FPGA	Field Programmable Gate Array.
GMII	Gigabit Media Independent Interface.
GPIO	General Purpose Input Output.
IC	Inter-integrated Circuit. A two wire low speed serial interface.
MAC	Media Access Control.
Magnetics	Commonly used to refer to the inductors and transformers within the Ethernet signalling to the RJ45 connector.
MCB	Memory Control Block. A Spartan 6 internal hard core.
MicroSD	Small form factor variant of SD.
PHY	Commonly used to refer to the device that interfaces to the physical layer.
PPS	Pulse Per Second. A high accuracy external clock input.
RAM	Random Access Memory.
RGMII	Reduced pin count GMII.
RJ45	Commonly used to refer to the 8-pin connector used in Ethernet communication.
SATA	Serial Advanced Technology Attachment. Refers to the high-speed serial signalling on hard disk drives.
SD	Secure Digital. Related to the format of some non-volatile memory cards.
SEIC	Sundance External Interface Connector.
SLB	Sundance Local Bus. Multiple 8-bit LVDS synchronous busses.
SoC	System on a Chip.
SPB	Sundance Platform Bus. 50-way connector with multiple LVDS signals.
SSB	Sundance SRIO Bus.
USB	Universal Serial Bus.
VGA	Video Graphics Array. Used here to refer to the analog portion of the video signal.

### 3 Block Diagram

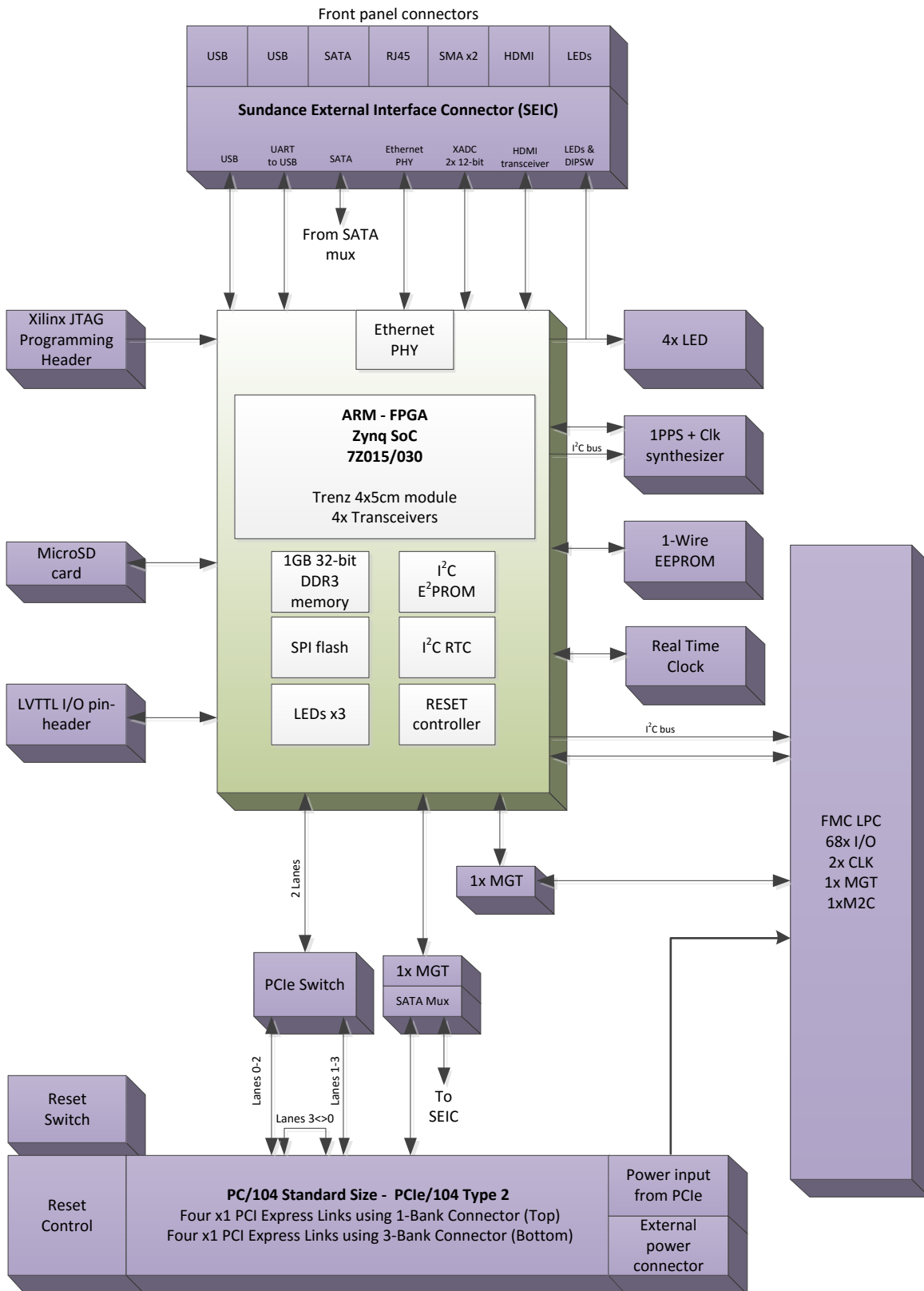


Figure 1: EMC2-Z7015/30 (with Zynq SoM and Break-out)

## 4 Circuit Description

The main component of the EMC<sup>2</sup>-DP is the SoM based module. Some versions includes the Zynq SoC, configuration device, Ethernet PHY and all power supply components necessary - with just a single 3.3V supply being required and others have the Artix-7 or the Kintex-7. Below is the Zynq variation.

Another feature of the EMC<sup>2</sup>-DP is the use of an expansion board to the PCIe/104 form-factor. This expansion board, (Sundance External Interface Connector = SEIC) module, contains most of the I/O connectors and in some cases, interface circuitry too. The SEIC module is connected to the main board using a 100-pin Samtec high density connector ([Razor Beam™](#)) similar to that used for the SoM module. When both boards are connected they lie in the same plane. See the PCB layout drawing for more details.

### 4.1 TE0715 FPGA ‘System-on-Module’

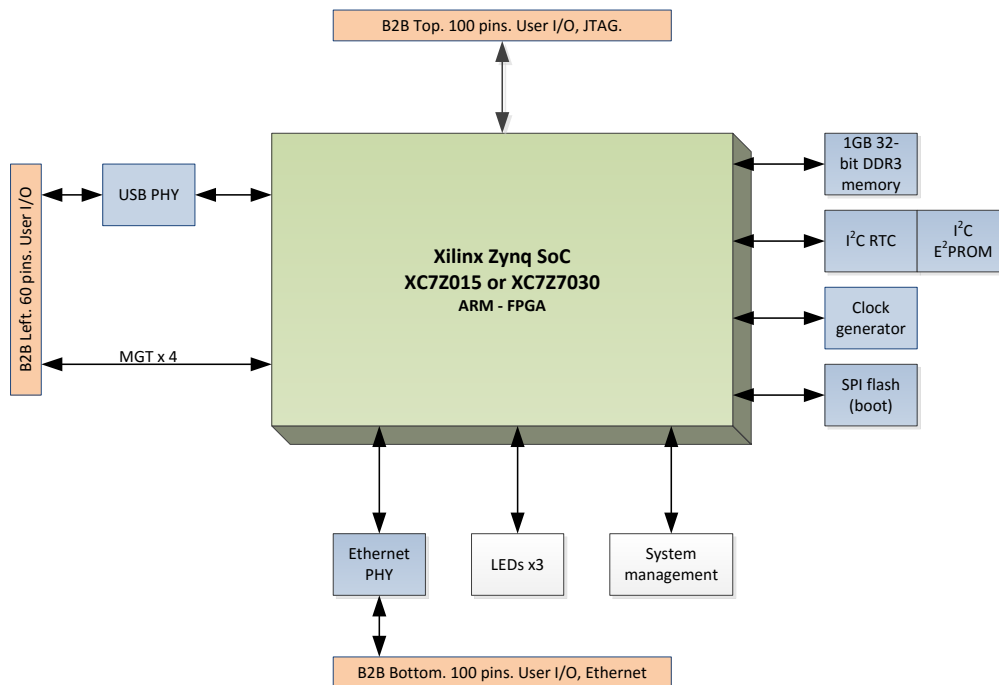


Figure 2 Block Diagram of the 40mm x 50mm SoM Module



Figure 3 Top of Trenez 40mm x 50mm SoM Module - 1:1 Format



### 4.1.1 FPGA

The Xilinx XC7Z015/Z7030 SoC incorporates a dual ARM A9 core running at up to 1GHz. The A9 based APU (Application Processor Unit) includes a 32kB level 1 cache and a 512kB level 2 cache. The level 1 caches are core independent but the level 2 cache is shared.

On-chip memory includes 256kB of RAM. This is supplemented by external memory interfaces which include DDR3, NOR and NAND flash.

Other peripherals include tri-speed Ethernet MAC, USB 2.0 OTG, CAN bus, SD controller, SPI, I<sup>2</sup>C, UARTs and GPIO pins.

Coupled to this PS (Processing System) is the PL (Programmable Logic). This is typical Xilinx FPGA architecture and includes block RAMs, DSP blocks, LUTs, flip-flops and adders. A total of 74k logic cells and 380kB of RAM are provided.

Programmable I/O blocks support many signalling schemes from 1.2 to 3.3V. Four high speed (6.25Gb/s) serial links are provided which can be used as a PCIe interface.

For full details about the Zynq SoC FPGA Family; See the [Xilinx website](#)

For full details regarding the Trenz TE0715 module; see [Trenz website](#), and [Trenz Wiki](#). This is [User Manual](#) for TE0715.

### 4.1.2 Local Power Supplies

A range of [Enpirion](#) DC-DC step-down converters are used to create the local voltages of 1.8V, 1.5V and 1.0V. These can supply 1.5A, 1.5A and 4A respectively.

### 4.1.3 Configuration and Booting

The SoC's configuration is volatile. When power is removed and then restored, the configuration is lost. Configuration of the device is typically performed using bitstreams stored in the SPI Flash device. The Trenz Wiki has [detailed explanation](#) of the boot process:

The basic procedure is as follows. The primary boot source is from the SoC SPI flash memory. Upon power-on, the Zynq will fetch the FSBL (first stage bootloader) from this device. This FSBL code initialises the peripherals and DDR3 memory, then proceeds to load object code for the PS and/or FPGA configuration data. Factory programmed FSBL does not have to configure the FPGA fabric.

The FSBL image cannot reside on the NAND flash; only on the SPI flash or external SD card.

The SSBL (second stage bootloader) is also usually stored in SPI flash. By default this loads a customised u-boot which is then responsible for loading the O/S. U-boot functionality is not essential and a user application could be directly loaded as an SSBL image.

The boot mode can be selected to be either JTAG (no boot), SPI flash, or external SD card.

The FPGA fabric can be loaded using u-boot or Linux (or JTAG).

### 4.1.4 JTAG

A 14-pin 2mm pitch pin header is provided for connection to a Xilinx USB Programmer (using the standard ribbon cable). This allows access to the internals of the SoC for configuration and debugging.

### 4.1.5 SoC Memory DDR3 in Zynq SoM

Two [16-bit wide DDR3 memory](#) devices are used on the SoM module to provide **1GByte** of storage. This memory is directly accessible by the dual ARM9 processor cores.

### 4.1.6 SPI Flash

This serially accessible device holds the configuration for the SoC. It is 32Mbytes in capacity and implemented using a [Winbond W25Q256FV](#) device.

The SPI flash can be programmed using Vivado 2013.4 (or later) but NOT via the Impact programming tool.

The SPI flash can also be re-programmed by the Zynq from files stored on the SD card. U-boot commands *fatload* and *sf* are used for this.

The SPI resides on the Zynq MIO bus bits 1..6.

### 4.1.7 SD Card

A microSD (transflash) socket can accept a memory card. This socket is part of the mainboard and not the TE0715 module.

The TE0715 can boot directly from the SD card (bypassing the SPI flash).

The SD interface resides on the Zynq MIO bits 40..45.

#### 4.1.8 I2C EEPROM

For smaller amounts of data, a separate non-volatile memory is provided which resides on an I<sup>2</sup>C bus made available from the SoC.

This device can be used to store operating parameters separate from the configuration Flash. E.g. MAC address.

This I<sup>2</sup>C interface resides on the Zynq MIO bits 48..49.

#### 4.1.9 RTC

Real time clock functionality is provided by an Intersil [ISL12020M RTC](#). This is backed-up with a 0.2F Super Cap in the event of power loss. This back-up lasts about 7 days and is located on the main board.

Allocated on MIO bits 0 and 47.

#### 4.1.10 LEDs

Three user LEDs are provided directly on the SoC module. These are in addition to any that are available on the EMC<sup>2</sup>-DP main circuit board.

#### 4.1.11 Interface Connectors

The SoC is attached to the main board using high density [Samtec connectors](#).

The pinout of these connectors is provided [here](#).

#### 4.1.12 Ethernet PHY

A single Ethernet PHY on the SoC ([Marvell 88E1512](#)) provides network connection on the SEIC via an RJ45 connector. This is a tri-mode device.

This interface resides on the Zynq MIO bits 16..27, 52, 53..

#### 4.1.13 USB

A Microchip [USB3320C](#) provides a full featured hi-speed USB interface. This interface is made available on the SEIC and thus through the rear enclosure panel.

This interface resides on the Zynq MIO bits 28..39, 51.

#### 4.1.14 MIO Allocation

MIO Pin	Peripheral	Signal
MIO 0	RTC	RTC_INT#
MIO 1	Quad SPI Flash	SPI-CS
MIO 2	Quad SPI Flash	SPI-DQ0/M0
MIO 3	Quad SPI Flash	SPI-DQ1/M1
MIO 4	Quad SPI Flash	SPI-DQ2/M2
MIO 5	Quad SPI Flash	SPI-DQ3/M3
MIO 6	Quad SPI Flash	SPI-SCK
MIO 7	Module LED	MIO7
MIO 8	Quad SPI Flash	SPI_SCK_FB
MIO 9	PCI host mode(Install JP12)	HOST#
MIO 10	I2C 0	I2C0_SCL
MIO 11	I2C 0	I2C0_SDA
MIO 12	I2C 1	I2C1_SCL
MIO 13	I2C 1	I2C1_SDA
MIO 14	USB UART 0	UART_TX
MIO 15	USB UART 0	UART_RX
MIO 16	Ethernet PHY	ETH_TXCK
MIO 17	Ethernet PHY	ETH_TXD0
MIO 18	Ethernet PHY	ETH_TXD1
MIO 19	Ethernet PHY	ETH_TXD2
MIO 20	Ethernet PHY	ETH_TXD3
MIO 21	Ethernet PHY	ETH_TXCTL
MIO 22	Ethernet PHY	ETH_RXCK
MIO 23	Ethernet PHY	ETH_RXD0
MIO 24	Ethernet PHY	ETH_RXD1
MIO 25	Ethernet PHY	ETH_RXD2
MIO 26	Ethernet PHY	ETH_RXD3

MIO 27	Ethernet PHY	ETH_RXCTL
MIO 28	USB OTG PHY	OTG_DATA4
MIO 29	USB OTG PHY	OTG_DIR
MIO 30	USB OTG PHY	OTG_STP
MIO 31	USB OTG PHY	OTG_NXT
MIO 32	USB OTG PHY	OTG_DATA0
MIO 33	USB OTG PHY	OTG_DATA1
MIO 34	USB OTG PHY	OTG_DATA2
MIO 35	USB OTG PHY	OTG_DATA3
MIO 36	USB OTG PHY	OTG_CLK
MIO 37	USB OTG PHY	OTG_DATA5
MIO 38	USB OTG PHY	OTG_DATA6
MIO 39	USB OTG PHY	OTG_DATA7
MIO 40	MicroSD	SD_CLK
MIO 41	MicroSD	SD_CMD
MIO 42	MicroSD	SD_D0
MIO 43	MicroSD	SD_D1
MIO 44	MicroSD	SD_D2
MIO 45	MicroSD	SD_D3
MIO 46	LED input to PS (module)	PHY_LED2
MIO 47	RTC	RTC_INT
MIO 48	Local I2C (module)	SCL
MIO 49	Local I2C (module)	SDA
MIO 50	Ethernet PHY	ETH_RST
MIO 51	USB OTG PHY	OTG_RST
MIO 52	Ethernet PHY	ETH_MDC
MIO 53	Ethernet PHY	ETG_MDIO

## 4.2 VITA57.1 FMC-LPC I/O Module

This LPC (low-pin count) variant provides 34 I/O and 2 clocks as differential pairs. I<sup>2</sup>C and JTAG signals are also present. Background information here. A pin-out is provided at the end of this document. [http://en.wikipedia.org/wiki/FPGA\\_Mezzanine\\_Card](http://en.wikipedia.org/wiki/FPGA_Mezzanine_Card)

## 4.3 Clock Synthesiser

This is a programmable device, via a serial interface from the SoC, that can generate a range of clocks. Several outputs are available and are connected to the clock capable pins of the SoC.

An SMA connector allows for an external clock input (shown as a 1PPS clock). Signal conditioning and filtering is provided as standard. This may be removed during build time to increase the frequency range. The external 1PPS clock must be an LVTTTL signal of 1.8V.

This I<sup>2</sup>C interface resides on the Zynq MIO bits 48..49.

## 4.4 SATA

The SoC provides 4 high speed serial interfaces, MGTs. One of these is connected to a [MAX4986](#) via the SEIC to a SATA multiplexer/switch. E.g:

The outputs from this switch go to a standard SATA connector on the SEIC (accessible through the enclosure rear panel) and the other to the PCIe connector. The PCIe connection allows a SATA HDD to be attached without cabling to a [PCIe/104 Harddisk Module](#). An appropriate IP core, like Sundance's [FC003-D](#) must be included within the Zynq fabric to allow the use of a SATA HDD.

## 4.5 USB

A [Microchip USB3320C](#) USB PHY is mounted directly on the SoC and drives the SEIC based USB connector (type A, USB host).

## 4.6 Ethernet

A single Ethernet PHY ([Marvell 88E1512](#)) provides network connection on the SEIC via an RJ45 connector. This is accessible through the enclosure rear panel.

It is a tri-mode (10/100/1000) device.

## 4.7 HDMI

Mounted on the SEIC module is an HDMI connector. An Analog Devices [ADV7511KSTZ-P](#) transmitter is employed to interface to the Zynq FPGA fabric. The interface to the ADV part includes:

- 24 data lines.
- Separate VSYNC and HSYNC.
- Single-ended clock input.
- Interrupt pin to Zynq.
- I2C Bus.
- SPDIF out.

Fabric IP is used to drive the HDMI signals.

## 4.8 ADC

The Zynq SoC includes dual ADCs. Refer to chapter 30 - [XADC Interface](#) of the Zynq TRM:

They are 12-bit 1MSPS converters and are driven from an analog multiplexer (internal to the Zynq). On the EMC<sup>2</sup>-DP these inputs are driven from two SMA connectors on the SEIC module.

The XADC system can also measure on-chip temperature and power supplies.

## 4.9 UART

A 2-wire (Rx and Tx) UART interface can be provided by the SoC. These two wires are converted to a USB interface using a [Silicon Labs CP2103GM](#) (or similar) device. This is then made available on the SEIC module. A standard USB micro to USB A cable can connect this to a host PC. OS drivers are readily available for this device.

This interface resides on the Zynq MIO bits 14-RX and 15-TX.

## 4.10 MEMS (Factory build option)

A [3-axis accelerometer](#) and magnetometer can be added on the main board. The pad corresponds to the MPU-9150 provided by InvenSense. The device resides on a second I<sup>2</sup>C bus.

This bus uses the Zynq MIO bits 10-SCL and 11-SDA.



#### 4.11 LEDs

Four LED signals are driven directly from the SoC via current limiting resistors. They are made available to drive LEDs on the main PCIe/104 card and also on the SEIC module.

The LEDs connected to the PL should be driven with an open-collector type output pin from the Zynq. Those connected to the MIO should be driven using 3.3V LVTTTL.

#### 4.12 TTL I/O

An 8 pin 2mm dual-in-line connector allows direct access to 4 SoC I/O pins. These have ESD (overvoltage and under-voltage) protection.

These pins support signal levels up to 1.8V only.

#### 4.13 Reset

The Zync can be reset either from a push button or from the PCIe/104 connector.

When operating in standalone mode, a power-on reset circuit replaces the PCIe/104 reset.

The SoC employs a CPLD device to control power sequencing, reset generation, and initial Zynq configuration. The CPLD is a [Lattice XO2-1200](#) and its design can be customised. The SC is part of the SoC JTAG chain. See the [following link](#) for operational details on this SC (System Controller):

Note that the functionality of the system reset pin to the SoC should be set to generate an interrupt and not a Zynq POR if a flash based OS is being used. This enables a proper OS shutdown to be performed.

#### 4.14 1-Wire EEPROM

A Dallas/Maxim 1-Wire interface EEPROM connects to the PL part of the Zynq. This is operated at 3.3V and hence requires a bi-directional voltage convertor (MAX3394) to connect to the 1.8V Zynq I/O.

## 4.15 Zynq SoC

This device has the following interface connectivity:

Interface	Description	Comment(s)	Main, SoC or SEIC
DDR3	Memory for ARM.	DDR3 bank 0.	SoC
Flash	Used for device configuration.		SoC
SDcard	MicroSD.	Direct connection to Zynq.	Main
I2C EEPROM		Direct connection to Zynq.	SoC
USB	Host interface.	Available on the SEIC via type A connector.	SoC & Main
SATA	SATA interface.	PCIe/104 DOWN connector and SEIC.	SEIC
PCIe	1-lane PCIe.	PCI express UP connector.	Main
PCIe	1-lane PCIe.	PCI express DOWN connector.	Main
JTAG	For ARM and FPGA.	Header for FPGA configuration and ARM.	Main
MGT	1-lanes of high-speed serial.	FMC connector.	Main
LED	4 LEDs.		Main & SEIC
Clock Synth	Programmable PLL.	Used for the ADC sample clock. External clock input for 1PPS use.	Main
TTL	LVTTL (3.3V) I/O.	General purpose I/O to header.	Main
FMC		LPC signals.	Main
Ethernet PHY		Available when using an FMC or SEIC.	SoC
XADC	Two channel 12-bit ADC.	Analog connectors on SEIC.	SoC & Main
HDMI		Available when using an SEIC with the ADV7511.	SEIC
I2C	Serial bus.	Used to interface to the clock generator, RTC, I2C Eprom, etc.	SoC
RTC	Real Time Clock		SoC
Switch	For general purpose use.	8-bit DIP SW.	Main & SEIC
UART	Uses a USB to RS232 convertor.	Available when using an SEIC with SI CP2103GM.	SEIC
SPI Flash	Serial flash.		SoC

## 4.16 PCIe

The EMC2-DP board can operate in both host and add-on board modes.

The PCIe/104 connectors provide power (+12V, +5V, +3V3), global Reset, and PCI express connections to the host from the FPGA. An external connector is used to provide +12V power as the 1-bank connector does not supply this voltage.

The FPGA site provides 2 MGT lanes which are routed as PCIe to two ports of a 6-lane, 6-port PCIe packet switch (PEX8606 from PLX). The other 4 ports are routed to a signal switch (PI3PCIE3442 from Pericom).

The following diagram shows the lane connectivity when in host mode:

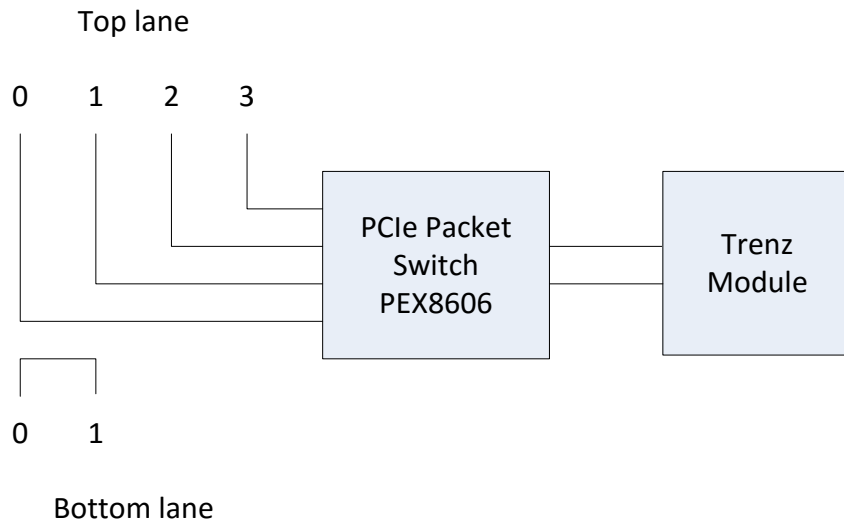


Figure 4 PCI Express Lanes in Host Mode

The effective loopback of bottom lanes 0 and 1 is a by-product of the signal switch operation. As the EMC2-DP is intended to form the base of the stack, this will have no consequence.

The following diagram shows the lane connectivity when in add-on mode:

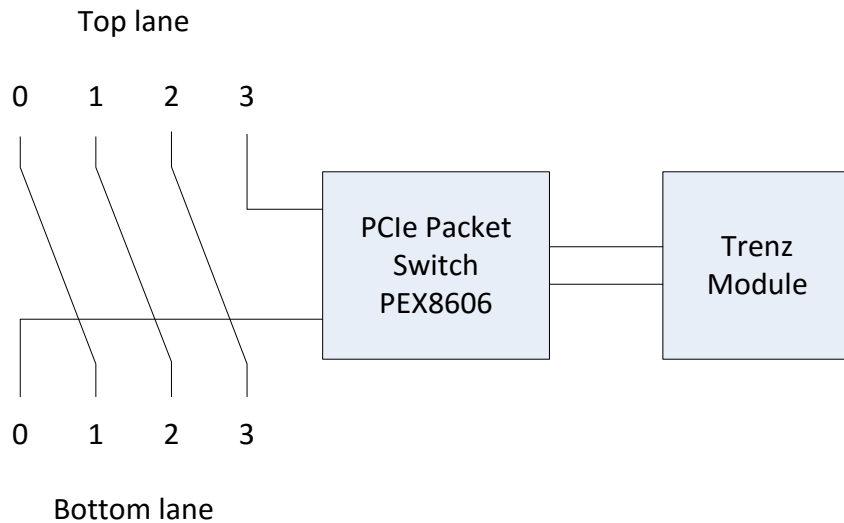


Figure 5 PCI Express Lanes in 'Add-On' Mode

As can be seen, the EMC2-DP can be used in either a stack-down or stack-up configuration.

The following diagram shows the lane connectivity as part of a stack:

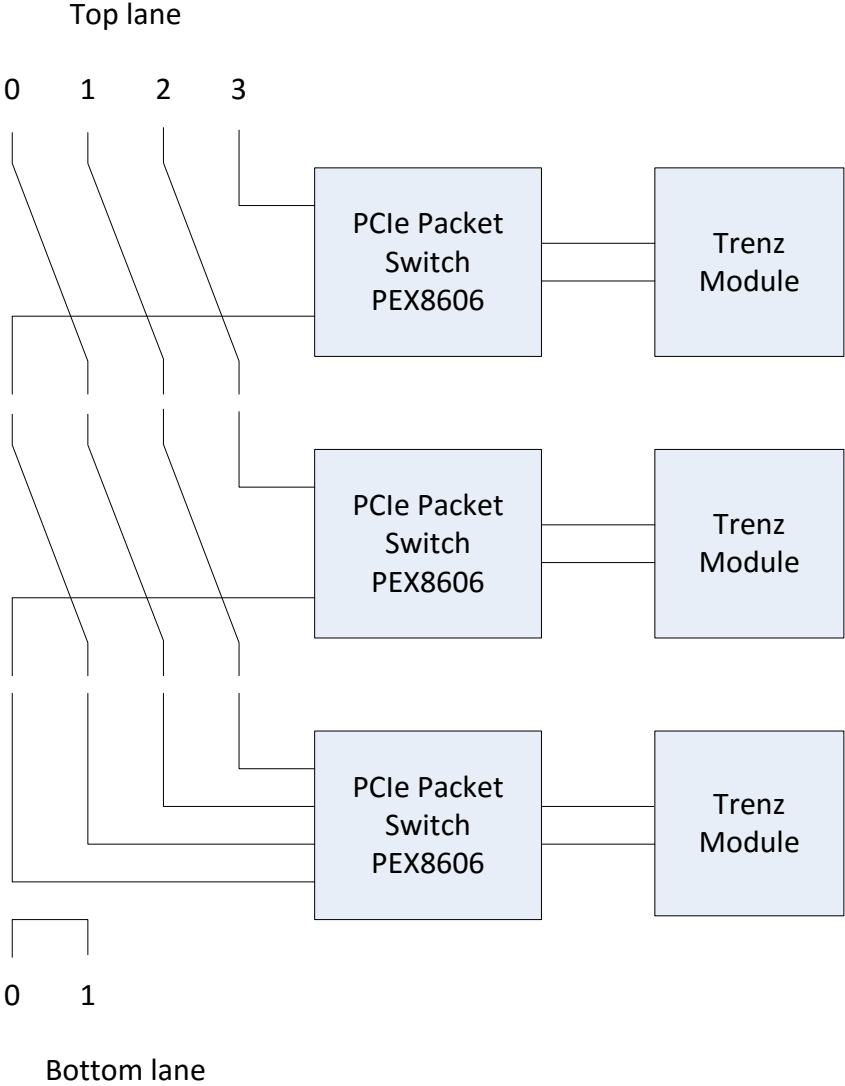
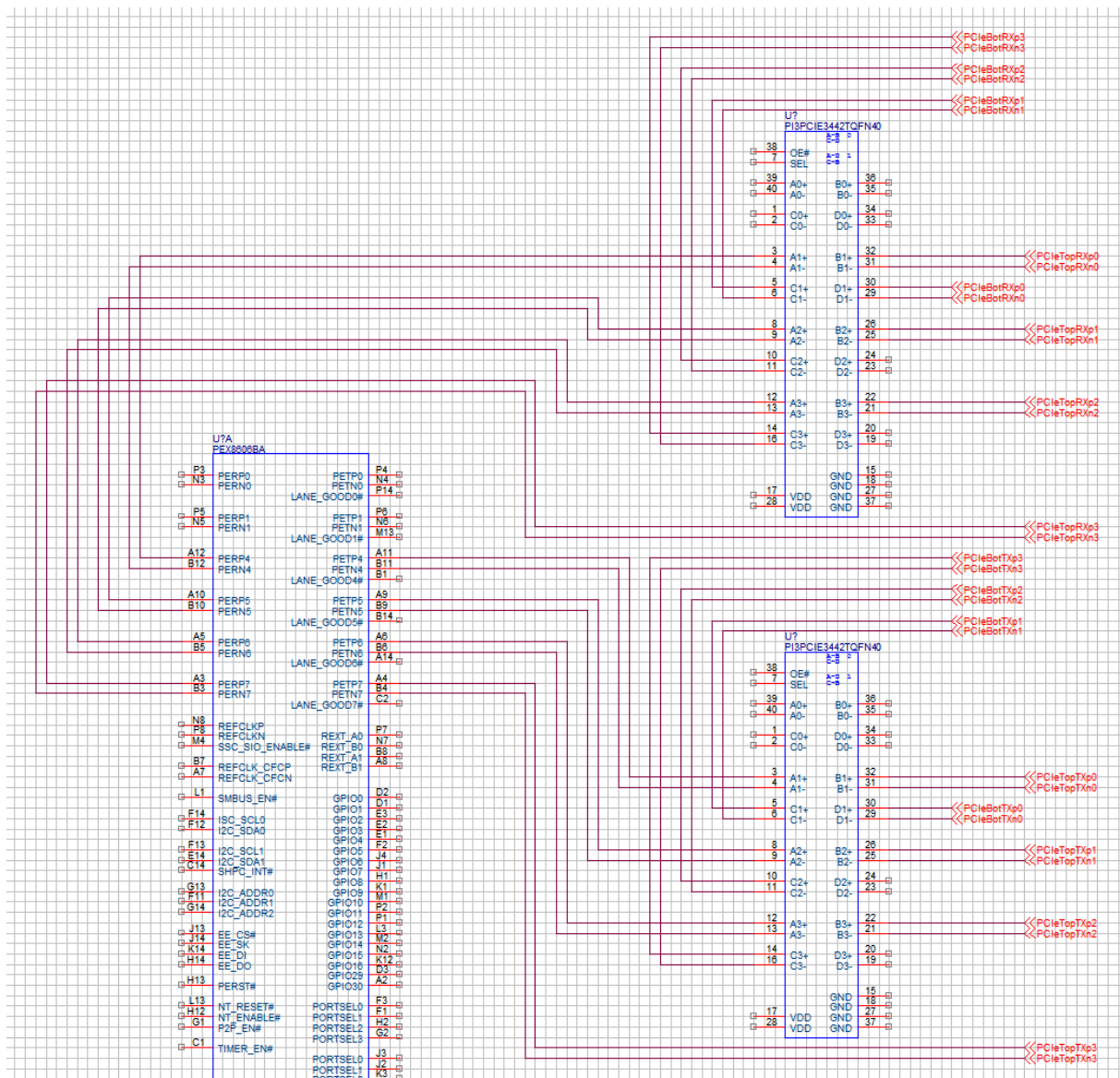


Figure 6 Multiple EMC<sup>2</sup>-DP in a PC/104 Stack

Two signal switches are required to route the PCIe lanes to the correct places. One switch for each of the Rx and Tx pairs.



The generation and routing of the PCIe reference clock is simpler. In host mode, a local oscillator is buffered and separate buffer outputs drive the four lanes to the top connector, the PCIe packet switch, and the Trenz module. The reference clocks to lanes 1-3 of the bottom connector are hardwired to the top lanes in the standard lane shift method. So, in host mode, 7 lanes are driven (not bottom lane 0 - which is unused in host mode).

In add-on mode, the buffer is disabled and hence the reference clock is sourced from either top lane 3 or bottom lane 0 via a selector that is switched using the CPU\_DIR signal.

## 5 JP7, JP8, JP7A, JP8A, JP6

There are three combinations to select different voltages in order to feed the I/O Banks of the FPGA.

For 3.3V : Set JP8 and JP7 to position 1-2.

For 1.8V : Set JP8 and JP7 to position 2-3.

For 2.5V : Set JP8 to position 2-JP8A, and JP7 to position 2-JP7A.

The jumper JP6 is a V33OUT bypass. Set it up to enable on-board components like the PEX switch to power up whether or not a Trenz module is installed; in other words, this jumper cuts the Trenz module out of the power-up sequence.

## 6 Board parts

The EMC<sup>2</sup>-DP is a PCIe/104 OneBank™ Form-Factor module without the "wing" extensions. The pictures below show the EMC<sup>2</sup>-DP and the front panel SEIC.

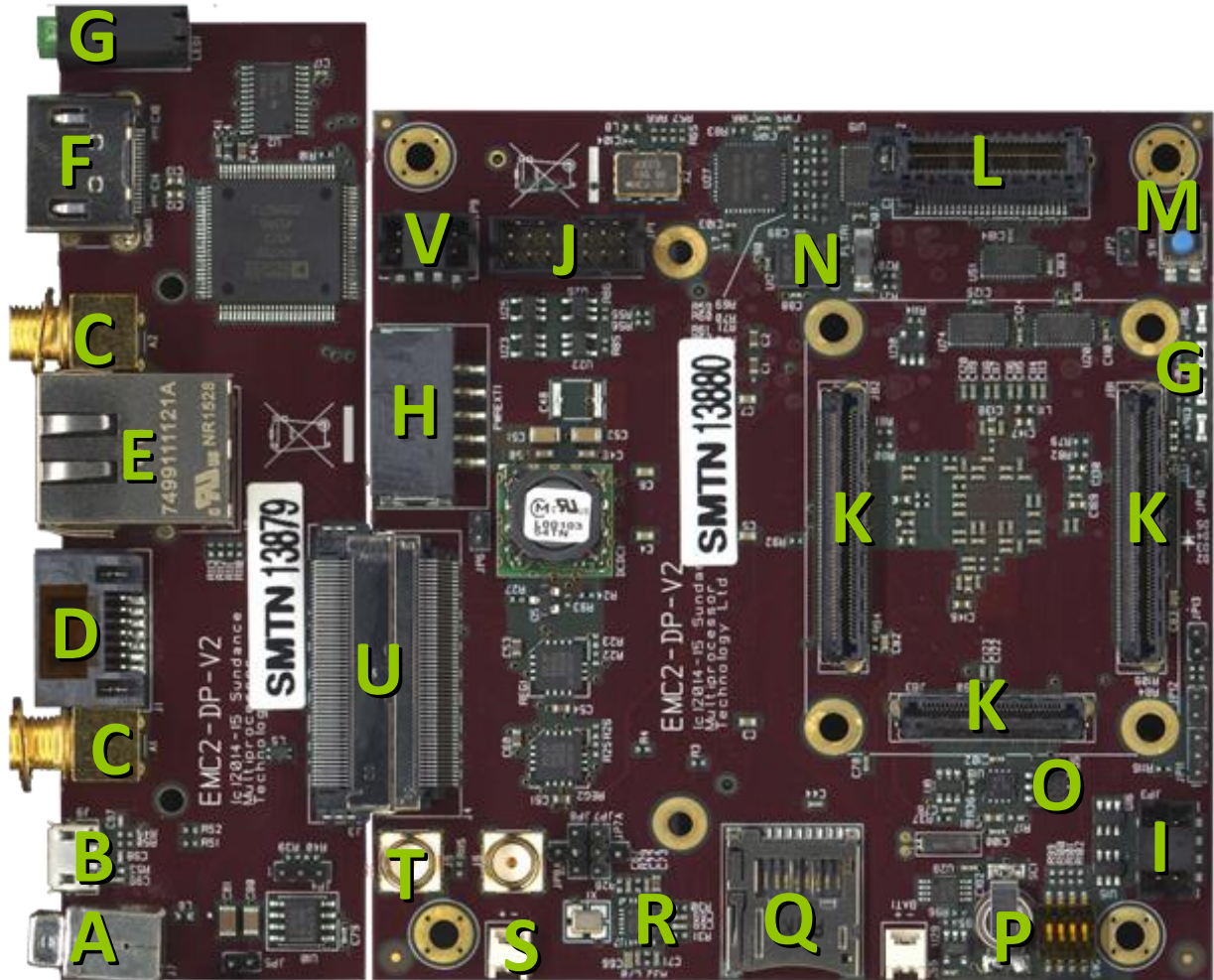


Figure 7 Top View of EMC<sup>2</sup>-DP

A - USB	L - PCIe/104 OneBank
B - UART	M - Reset button
C - SMA	N - SATA Switch
D - SATA	O - 1-Wire Device
E - RJ45	P - Battery backup
F - HDMI	Q - Micro SD
G - LEDs	R - Clock synthesizer
H - External Power	S - Fan connector
I - TTL I/O	T - Clock in
J - Xilinx JTAG	U - External I/O (SEIC)
K - 40mm x 50mm SoM	V - FMC JTAG

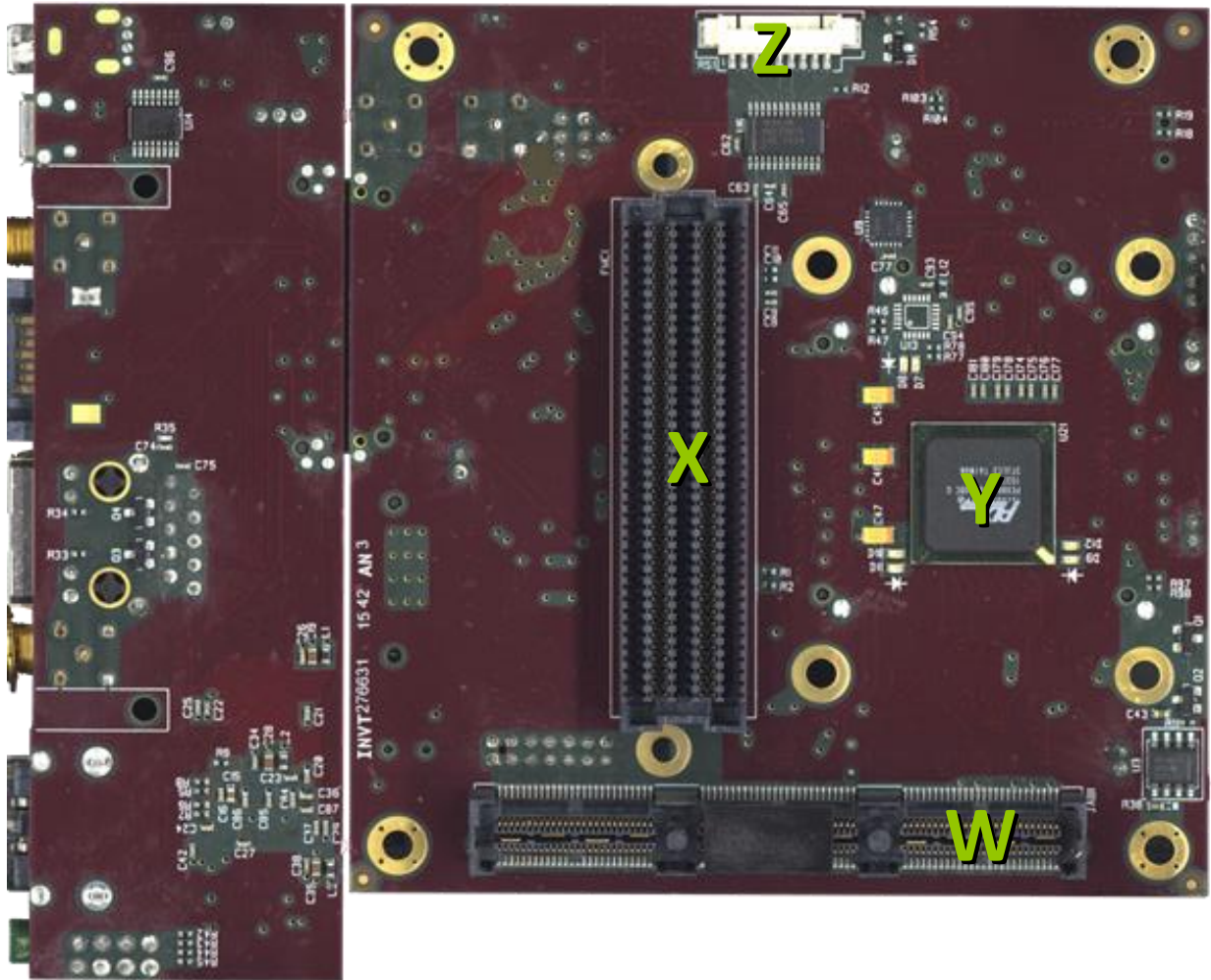


Figure 8 Bottom View of EMC²-DP

- W - PCIe Stack
- X - FMC
- Y - PCIe Switch
- Z - RS232



## 7 Physical Properties

Dimension, PC/104	90mm	96mm
Dimension, SEIC	33mm	106mm

Weight	
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Voltage	Power (estimate)

RH	10-80%
Temperature	-10 to +40°C -25 to +80°C

MTBF	> 50,000 hours
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## 8 FMC Pin-Out

FMC pin	Signal	Trenz pin	FMC pin	Signal	Trenz pin
C1	GND	-	C21	GND	-
C2	FMC_TRZ_TX_P	JB3.26	C22	FMC_LA18_P	JB2.52
C3	FMC_TRZ_TX_N	JB3.28	C23	FMC_LA18_N	JB2.54
C4	GND	-	C24	GND	-
C5	GND	-	C25	GND	-
C6	FMC_TRZ_RX_P	JB3.25	C26	FMC_LA27_P	JB2.76
C7	FMC_TRZ_RX_N	JB3.27	C27	FMC_LA27_N	JB2.78
C8	GND	-	C28	GND	-
C9	GND	-	C29	GND	-
C10	FMC_LA06_P	JB1.45	C30	FMC_SCL	JB1.32
C11	FMC_LA06_N	JB1.47	C31	FMC_SDA	JB1.34
C12	GND	-	C32	GND	-
C13	GND	-	C33	GND	-
C14	FMC_LA10_P	JB1.59	C34	GA0	-
C15	FMC_LA10_N	JB1.61	C35	V12P	-
C16	GND	-	C36	GND	-
C17	GND	-	C37	V12P	-
C18	FMC_LA14_P	JB1.69	C38	GND	-
C19	FMC_LA14_N	JB1.71	C39	V33FMC	-
C20	GND	-	C40	GND	-

FMC pin	Signal	Trenz pin	FMC pin	Signal	Trenz pin
D1	V33FMC	-	D21	FMC_LA17_N	JB2.57
D2	GND	-	D22	GND	-
D3	GND	-	D23	FMC_LA23_P	JB2.71
D4	FMC_TRZ_CK_P	JB3.31	D24	FMC_LA23_N	JB2.73
D5	FMC_TRZ_CK_N	JB3.33	D25	GND	-
D6	GND	-	D26	FMC_LA26_P	JB2.66
D7	GND	-	D27	FMC_LA26_N	JB2.68
D8	FMC_LA01_P	JB1.66	D28	GND	-
D9	FMC_LA01_N	JB1.68	D29	FTCK	-
D10	GND	-	D30	FTDI	-
D11	FMC_LA05_P	JB1.49	D31	FTDO	-
D12	FMC_LA05_N	JB1.51	D32	V33OUT	-
D13	GND	-	D33	FTMS	-
D14	FMC_LA09_P	JB2.42	D34	FTRST	-
D15	FMC_LA09_N	JB2.44	D35	GA1	-
D16	GND	-	D36	V33FMC	-
D17	FMC_LA13_P	JB1.70	D37	GND	-
D18	FMC_LA13_N	JB1.72	D38	V33FMC	-
D19	GND	-	D39	GND	-
D20	FMC_LA17_P	JB2.55	D40	V33FMC	-

FMC pin	Signal	Trenz pin	FMC pin	Signal	Trenz pin
G1	GND	-	G21	FMC_LA20_P	JB2.48
G2	FMC_CLK1_P	JB1.65	G22	FMC_LA20_N	JB2.46
G3	FMC_CLK1_N	JB1.67	G23	GND	-
G4	GND	-	G24	FMC_LA22_P	JB2.61
G5	GND	-	G25	FMC_LA22_N	JB2.63
G6	FMC_LA00_P	JB1.76	G26	GND	-
G7	FMC_LA00_N	JB1.78	G27	FMC_LA25_P	JB2.75
G8	GND	-	G28	FMC_LA25_N	JB2.77
G9	FMC_LA03_P	JB1.46	G29	GND	-
G10	FMC_LA03_N	JB1.48	G30	FMC_LA29_P	JB2.81
G11	GND	-	G31	FMC_LA29_N	JB2.83
G12	FMC_LA08_P	JB1.56	G32	GND	-
G13	FMC_LA08_N	JB1.58	G33	FMC_LA31_P	JB2.85
G14	GND	-	G34	FMC_LA31_N	JB2.87
G15	FMC_LA12_P	JB1.36	G35	GND	-
G16	FMC_LA12_N	JB1.38	G36	FMC_LA33_P	JB2.95
G17	GND	-	G37	FMC_LA33_N	JB2.97
G18	FMC_LA16_P	JB2.72	G38	GND	-
G19	FMC_LA16_N	JB2.74	G39	VCCIO35	
G20	GND	-	G40	GND	-

FMC pin	Signal	Trenz pin	FMC pin	Signal	Trenz pin
H1	FMC_VREF	-	H21	GND	-
H2	PRSNT_M2C_L	JB2.37	H22	FMC_LA19_P	JB2.51
H3	GND	-	H23	FMC_LA19_N	JB2.53
H4	FMC_CLK0_P	JB1.60	H24	GND	-
H5	FMC_CLK0_N	JB1.62	H25	FMC_LA21_P	JB2.65
H6	GND	-	H26	FMC_LA21_N	JB2.67
H7	FMC_LA02_P	JB1.35	H27	GND	-
H8	FMC_LA02_N	JB1.37	H28	FMC_LA24_P	JB2.82
H9	GND	-	H29	FMC_LA24_N	JB2.84
H10	FMC_LA04_P	JB1.50	H30	GND	-
H11	FMC_LA04_N	JB1.52	H31	FMC_LA28_P	JB2.86
H12	GND	-	H32	FMC_LA28_N	JB2.88
H13	FMC_LA07_P	JB1.55	H33	GND	-
H14	FMC_LA07_N	JB1.57	H34	FMC_LA30_P	JB2.91
H15	GND	-	H35	FMC_LA30_N	JB2.93
H16	FMC_LA11_P	JB1.39	H36	GND	-
H17	FMC_LA11_N	JB1.41	H37	FMC_LA32_P	JB2.99
H18	GND	-	H38	FMC_LA32_N	JB2.90
H19	FMC_LA15_P	JB1.75	H39	GND	-
H20	FMC_LA15_N	JB1.77	H40	VCCIO35	-

## 9 Trenz Module Pin-Out & Schematics

Download full schematic [from here](#) and the reference designs from [here](#)  
Verification, Review & Validation Procedures

To be carried out in accordance with the [Sundance Quality Procedures](#) (ISO9001).

## 10 Safety

This module presents no hazard to the user when in normal use.

## 11 EMC

This module is designed to operate from within an enclosed host system, which is built to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate enclosure.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.

## 12 Ordering Information

Order number:

<b>EMC<sup>2</sup>-SoM</b>	No SoM Module; No SEIC expansion
<b>EMC<sup>2</sup>-DP</b>	No SoM Module; SEIC expansion
<b>EMC<sup>2</sup>-Z7015-y</b>	Zynq Z7015 SoC FPGA
<b>EMC<sup>2</sup>-Z7030-y</b>	Zynq Z7030 SoC FPGA
<b>EMC<sup>2</sup>-7A100-y</b>	Artix-A100 FPGA
<b>EMC<sup>2</sup>-7A200-y</b>	Artix-A200 FPGA
<b>EMC<sup>2</sup>-7K070-y</b>	Kintex-K070 FPGA
<b>EMC<sup>2</sup>-7K160-y</b>	Kintex-K160 FPGA
<b>EMC<sup>2</sup>-7K325-y</b>	Kintex-K325 FPGA
<b>EMC<sup>2</sup>-7K410-y</b>	Kintex-K410 FPGA

y:

C = Commercial temperature

I = Industrial temperature