Unit / Module Description:	PCIe/104 OneBank + ARM + FPGA + FMC carrier
Unit / Module Number:	EMC²-DP V2
Document Issue Number:	1.0_z712-15-30
Original Issue Date:	17/03/2016
Original Author:	Timoteo Garcia

EMC²-DP
BOARD IO

PCIe/104 OneBank™ Carrier for 40mm x 50mm SoM + VITA57.1 FMC™ Modules

Sundance Multiprocessor Technology Ltd,
Chiltern House, Waterside, Chesham, Bucks, HP5 1PS, UK.

Revision History

Version	Date	Initials	Changes
v1.0	17/03/2016	TG	First released version. Covers V2 boards with TE0715 & TE0730 and TE0712 modules.
			Includes a tab populated with the master pinout spreadsheet from Trenz.

Table of Contents

Table of Contents

1 Board parts

The EMC²-DP is a PCIe/104 OneBank™ Form-Factor module without the "wing" extensions. The pictures below show the EMC²-DP and the front panel SEIC.

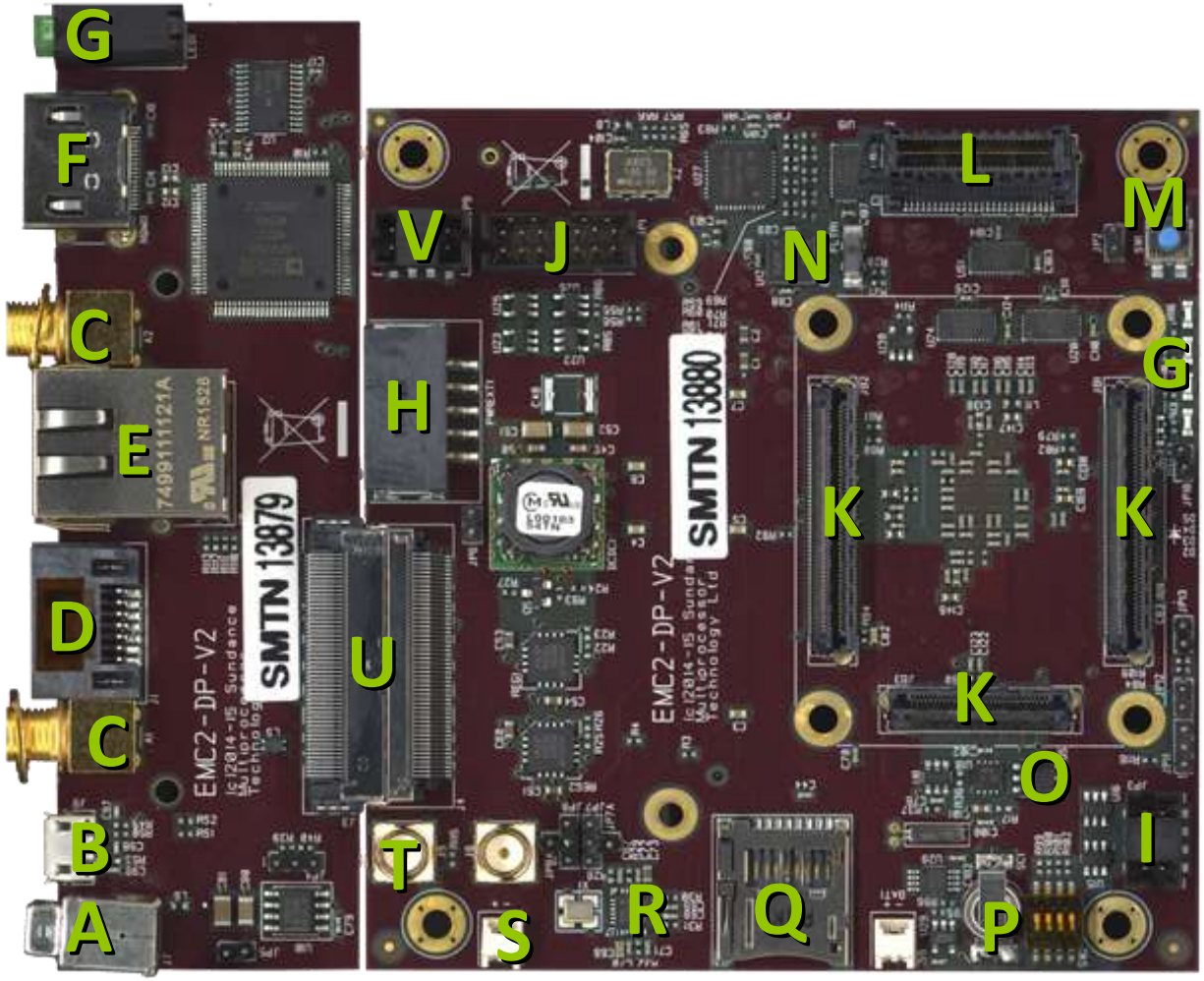

Figure 1 Top View of EMC²-DP

A - USB
B - UART
C - SMA
D - SATA
E - RJ45
F - HDMI
G – LEDs
H – External Power
I - TTL I/O
J - Xilinx JTAG
K - 40mm x 50mm SoM
L - PCIe/104 OneBank
M - Reset button
N - SATA Switch
O - 1-Wire Device
P - Battery backup
Q - Micro SD
R - Clock synthesizer
S - Fan connector
T - Clock in
U - External I/O (SEIC)
V - FMC JTAG

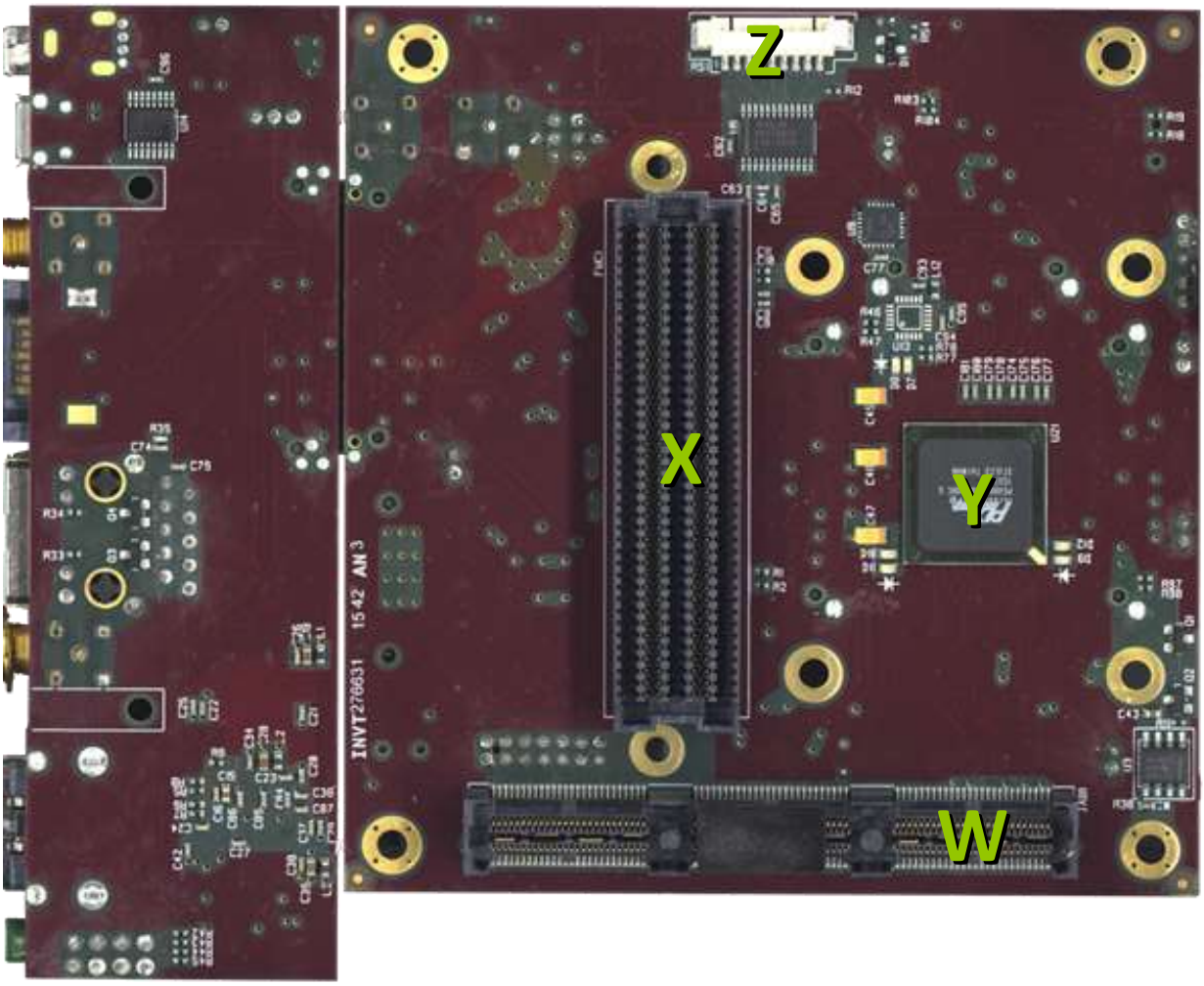

Figure 2 Bottom View of EMC²-DP

W - PCIe Stack
X - FMC
Y - PCIe Switch
Z - RS232

2 Overview

This document describes the IO functionalities of the EMC2-DP, as a reference for the user, providing the information related to the different modules and versions of the board.

1. Devices local to the Trenz module. Local I2C is connected to MIO 48,49 (Zynq I2C1 mappable) and is not routed off-module	
TE0715	
	S25FL256S 32MB QSPI boot flash
I^{2}C 0x50	Microchip 24AA025E48 – 2kbit NVM + MAC
I^{2}C 0x6F	ISL12020 RTC – receives VBAT from carrier; not present on TE0715-01-XX-XX
I^{2}C 0x70	SI5338A clock synthesizer; default output 125MHz for MGT reference clock #1
	USB3320C USB PHY (for USB OTG) – connector signals routed to carrier
	88E1512 Ethernet PHY – connector signals routed to carrier.
	LCMX02-256HC system CPLD – not directly accessible from Zynq, no I2C interface, some control signals routed to carrier
2. EMC2-DP and SEIC devices and I/O	
EMC2-DP	
	MicroSD slot with card-present switch
	DS2432 1-wire secure NVM with SHA -1 engine and unique ID
I^{2}C[0] 0x50	Microchip 24AA02E64 – 2kbit NVM + MAC
I^{2}C[0] 0x68	DS1337 RTC
I^{2}C[0] 0x70	SI5338A clock synthesizer
	SATA (or general purpose MGT), routed to the SEIC or PCIe/104 stack-down connector
I^{2}C[0] 0x3A	PEX8606 PCI Express packet switch (with LED 3 and 4 on GPIO)
PCIe/104	
	I^{2}C[1] routed to PCIe/104 SMB pins
	4 PCIe lanes routed from PEX8606 to stack-up connector in Host mode
	1 lane routed from PEX8606 to stack-down connector and 1 to stack-up connector in Peripheral mode
	SATA lane on stack-down connector can have an MGT routed to it
SEIC	
I^{2}C[0] 0x39	ADV7511 HDMI transmitter and TPD12S016 companion device
I2C addresses are specified in the ADV7511 documentation as if they occupied the top 7 bits of a byte, i.e. an address of 0x72 in the documentation implies a value of 0x39 in the 7-bit address field. This is a different I2C bus from that on the Trenz module, but uses the same PS peripheral. By default the ADV7511 also responds to 0x70 (Packet memory), 0x7E (EDID memory), and 0x78 (CEC memory). These are "normal" I2C addresses of 0x38, 0x3F, and 0x3C	

	RJ45 Ethernet connector
	USB OTG connector (USB-A)
	SATA connector
FMC	
No FMC module functionality pre-defined; however FPGA to FMC pin mapping is documented	
3. Jumpers	
JP2	If installed, holds board in reset
JP4 [on SEIC]	Select USB VBUS sense series resistor - position 1-2 for 1000 ohm, position 2-3 for 10000 ohm
JP5 [on SEIC]	USB VBUS power. To provide USB power, install jumper and configure the USB PHY for OTG mode.
JP6	V33OUT bypass. Install to enable on-board components like the PEX switch to power up whether or not a Trenz module is installed.
JP7(A)	FPGA I/O voltage A (SEIC HDMI). **MUST BE INSTALLED BEFORE APPLYING POWER TO THE BOARD.**
	Set to position 1-2 for 3.3V, position 2-3 for 1.8V, 2-JP7A for 2.5V.
	TE0712 Artix module: Bank 13
	TE0715 Zynq module: Bank 34
JP8(A)	FPGA I/O voltage B (FMC). **MUST BE INSTALLED BEFORE APPLYING POWER TO THE BOARD.**
	Set to position 1-2 for 3.3V, position 2-3 for 1.8V, 2-JP8A for 2.5V.
	TE0712 Artix module: Bank 15
	TE0715 Zynq module: Banks 13 & 35
JP10	SATA routing (default SEIC) - install this jumper to route SATA to the PCIe stack-down connector
JP11	Boot Mode. Set to position 1-2 for boot from QSPI flash, position 2-3 (closest to JP12) for boot from SD card.
JP12	Host mode (default PCIe Peripheral mode) - install jumper to configure the EMC2 board as PCIe Root Complex for stack-up operation.
JP13	Test point exposing PEX8606 INTA# and FATAL_ERR#
SW1	Reset pushbutton
SW2	PEX8606 Upstream Port selection.
	All On: LLLL = Port 0 - Zynq (PEX8686 lanes 0 and 1) - use for Host mode
	Off-On-On-On: LLLH = Port 1 - PCIe stack-up or stack-up lane 0(PEX8606 lane 4) - use for stack-up Peripheral mode. For this mode, only the switch nearest the mounting hole is ON.
	LHLH = Port 5 - PCIe stack-up lane 1 (PEX8606 lane 5) - N/C in Peripheral mode
	LHHH = Port 7 - PCIe stack-up lane 2 (PEX8606 lane 6) - N/C in Peripheral mode
	Off-On-On-Off: HLLH = Port 9 - PCIe stack-up lane 3 (PEX8606 lane 7) - use for stack-down Peripheral mode
4. Connectors	
EMC2-DP	
BAT1	Battery input for carrier RTC and (if fitted) module RTC
FAN1	Unlabelled, adjacent to J6. +5V and GND for a fan if one is required.

J2	PCIe/104 OneBank stack-up connector
J4	Sundance External I/O Connector for custom external peripheral module
J5	Pulse-per-second clock input. Apart from protection circuitry, goes via a 1k0 resistor to an FPGA input, and is therefore not limited to PPS applications.
J6	External clock, routed to IN3 of the on-board Si5338A clock synthesiser.
JAB1	PCIe/104 stack-down connector
JP1	14-pin JTAG header for Trenz module
JP3	LVTTL header with protection circuitry
	Pins 1 and 2 form a differential pair (un-terminated)
	Pin 3 supplies the voltage selected by JP7, pin 4 is GND
	Pin pairs (5,6) and (7,8) can be used as differential inputs with 100 ohm termination.
JP9	8-pin JTAG header for FMC module
PWREXT1	External power connector: pin order +12V, 5V, 3.3V, GND, N/C
	In a PCIe/104 stack, the board receives 3.3V and 5V via stacking connectors, and external power is only required if the installed FMC module requires +12V.
RS1	RS232 connector. True RS232 signal levels are supported, NOT logic-levels.
	Can be used as 3 simple RS232 ports without control signals, or one COM port with
	RTS/CTS and DTR/DSR.
SEIC module	
A1, A2	Analogue inputs (single ended), connected directly to an FPGA analogue input pins
HDMI	HDMI
J1	SATA
J3	SEIC connector to Trenz carrier board
J7	USB 2.0 on-the-go
J8	Ethernet RJ45 (all 8 conductors, suitable for gigabit Ethernet depending on Trenz module PHY)
J9	USB-serial connector, allows module to communicate with a development PC using a UART on the module and USB on the PC.

3 IO Voltages

Module pin	TE0712	TE0715	Board pin	EMC2-DP V1	EMC2-DP V2	EMC2-DP signal name
JM1 9 + JM1 11	VCCIO16	VCCIO13	JB1 10 + JB1 12	JP8	JP8	VCCIO35
JM2 1 + JM2 3	VCCIO13	N/C	JB2 2 + JB2 4	N/C	JP7	VCCIO34
JM2 5	N/C	VCCIO34	JB2 6	JP7	JP7	VCCIO34
JM2 7 + JM2 9	VCCIO15	VCCIO35	JB2 8 + JB2 10	JP8	JP8	VCCIO35

3.1 TE0715 & TE0730

Bank	MIO0_500	MIO1_501	13	34	35
Voltage	3.3V	1.8V	JP8	JP7	JP8
Usage	I2C0, I2C1	Ethernet PHY	FMC	HDMI	FMC
	HOST#	USB PHY	SD card present	HDMI companion	RS232 RX 2 & 3
	SEIC UART	SD	LED 1, 2	RS232	PCIeRST#
	QSPI flash	module I2C		TTL, PPS	Clock synthesizer
				1-wire	SEIC analogue

The pins related to the Bank 13 in the TE0730 module are High Range, and the pins related to the Bank 35 are High Performance. This can affect when powering the Banks with standards like LVDS 25. For more information, read the AR43989 from Xilinx.

3.2 TE0712

Bank	13	14	15	16	34	35
Voltage	N/C	3.3V	JP8	JP8	1.5V	1.5V
Usage	SD	HDMI companion	FMC	FMC	DDR3 RAM	DDR3 RAM
	HDMI	HDMI I2C, INT	SEIC analogue	LED 1, 2		
	RJ45	SEIC UART	RS232 RX 2 & 3	PHY LEDs		
		RS232	PCIeRST#	SD card present		
		TTL, PPS	Clock synthesizer			
		1-wire				
		I2C0, I2C1				
		RTC interrupt				
		HOST#				
		SEIC utility				

4 TE0715 & TE0730

Local devices of the Trenz module.
Local I2C is connected to MIO 48,49 and is not routed off-module

Peripheral Pin	Module Signal Name	Module pin	FPGA IO name	FPGA Pin
QSPI Flash				
CS	SPI-CS		MIO1	
SCK	SPI-SCK		MIO6	
SCK Feedback	SPI_SCK_FB		MIO8	
DQ0	SPI-DQ0/M0		MIO2	
DQ1	SPI-DQ1/M1		MIO3	
DQ2	SPI-DQ2/M2		MIO4	
DQ3	SPI-DQ3/M3		MIO5	
NVM + MAC				
[on local I2C]				
Local I2C				
This I2C bus is local to the module				
SCL	SCL		MIO48	
SDA	SDA		MIO49	
USB OTG PHY				
See USB OTG below for USB PHY pin assignments on EMC2-DP carrier				
	OTG_DIR		MIO29	
	OTG_STP		MIO30	
	OTG_NXT		MIO31	
	OTG_CLK		MIO36	
	OTG_DATA0		MIO32	
	OTG_DATA1		MIO33	
	OTG_DATA2		MIO34	
	OTG_DATA3		MIO35	
	OTG_DATA4		MIO28	
	OTG_DATA5		MIO37	
	OTG_DATA6		MIO38	
	OTG_DATA7		MIO39	
	OTG_RST		MIO51	
Ethernet PHY				
Ethernet PHY signals are routed to RJ45 or SFP transceiver on the carrier board				
	ETH_TXCK		MIO16	

	ETH_TXD0		MIO17	
	ETH_TXD1		MIO18	
	ETH_TXD2		MIO19	
	ETH_TXD3		MIO20	
	ETH_TXCTL		MIO21	
	ETH_RXCK		MIO22	
	ETH_RXD0		MIO23	
	ETH_RXD1		MIO24	
	ETH_RXD2		MIO25	
	ETH_RXD3		MIO26	
	ETH_RXCTL		MIO27	
	ETH_RST		MIO50	
	ETH_MDC		MIO52	
	ETH_MDIO		MIO53	
	PHY_LED0 (To CPLD)		-	
	PHY_LED1 (To CPLD)		-	
	PHY_LED2 (LED output from PHY, input to PS)		MIO46	
Clock Synth				
[on local I2C] The CLKIN2 differential signal comes from the carrier (JB3 pins 31 and 33 on the carrier) It is intended as a reference clock for MGTs. 25MHz crystal connected to IN3 (IN4 to ground) Signal is capacitively coupled between synthesizer and FPGA, and changes name from CLK2_P to MGT_CLK1_P and CLK2_N to MGT_CLK1_N Defaults to 125MHz				
IN1	CLKIN2_N	JM2 34	-	
IN2	CLKIN2_P	JM2 32	-	
IN3	unnamed		-	
CLK2A	CLK2_P / MGT_CLK1_P		MGTREFCLK1P_112	
CLK2B	CLK2_N / MGT_CLK1_N		MGTREFCLK1N_112	
RTC				
nIRQ	RTC_INT		MIO47	
SC CPLD				
PR5A_PCLKT1_0	X0		IO_L1N_T0_34	K8
PR5B_PCKLC1_0	X1		IO_L3P_T0_DQS_PUDC_B_34	K7
Misc				
Green LED on module				
Module LED	MIO7		MIO7	

5 TE0715 & TE0730 EMC2-DP and SEIC

5.1 TE0715 & TE0730 - EMC2-DP Peripherals

Peripheral Pin	Off-board pin	EMC2-DP signal	Carrier Trenz pin	Module signal	FPGA pin	FPGA IO name
MicroSD						
CLK	-	SD_CLK	JB1 28	MIO40		
CMD	-	SD_CMD	JB1 26	MIO41		
D0	-	SD_D0	JB1 24	MIO42		
D1	-	SD_D1	JB1 22	MIO43		
D2	-	SD_D2	JB1 20	MIO44		
D3	-	SD_D3	JB1 18	MIO45		
Card present sw	-	SD_SW	JB1 42	B12_L2_P	V15	IO_L2P_T0_13
DS2432 SHA NVM + ID						
DS2432 is a Dallas 1-wire protected NVM with SHA-1 engine and 1kbit storage. Connected via a MAX3394 level translator						
1-WIRE	-	WIRE1	JB2 36	B34_L7_P	J5	IO_L7P_T1_34
NVM + MAC						
[on I2C 0]						
DS1337 RTC						
[on I2C 0]						
nINTA		RTC_INT#	JB1 88	MIO0		
Clock Synthesiser – SI5338A						
[on I2C 0] Configured via I2C0 J6 is connected to IN6 of the SI5338 25MHz crystal connected to IN1/IN2						
CLK0A	-	CLK1	JB2 47	B35_L13_N	B3	IO_L13N_T2_MRCC_35
CLK1A	-	CLK2	JB2 45	B35_L13_P	B4	IO_L13P_T2_MRCC_35
CLK2A	-	CLK3	JB2 43	B35_L15_P	A2	IO_L15P_T2_DQS_AD12P_35
NOT a clock capable pin, but can be used with set_property CLOCK_DEDICATED_ROUTE FALSE						
CLK3A	-	CLK4	JB2 41	B35_L15_N	A1	IO_L15N_T2_DQS_AD12N_35
NOT a clock capable pin						
IN1	-	-	-	-		
IN2	-	-	-	-		
IN3	J6	unnamed	-	-		
I2C [0]						
SCL	-	I2C0_SCL	JB1 96	MIO10		
SI5338A clock synthesizer, DS1337 RTC, 24AA02E64 MAC address + NVM, MPU-9150 motion tracking device, PEX8606 PCIe switch						
SDA	-	I2C0_SDA	JB1 94	MIO11		

I2C [1]						
SCL	-	I2C1_SCL	JB1 100	MIO12		
PCIe SMB						
SDA	-	I2C1_SDA	JB1 98	MIO13		
SATA						
TX_P	[SEIC 23]	SATA_TRZ_TX_P	JB3 22	MGT_TX2_P	AA5	MGTTXP2_112
TX_N	[SEIC 21]	SATA_TRZ_TX_N	JB3 20	MGT_TX2_N	AB5	MGTTXN2_112
RX_P	[SEIC 24]	SATA_TRZ_RX_P	JB3 21	MGT_RX2_P	AA9	MGTRXP2_112
RX_N	[SEIC 22]	SATA_TRZ_RX_N	JB3 19	MGT_RX2_N	AB9	MGTRXN2_112
PCIe Reset						
Level-shifted, this PCIe reset signal from the stack-down connector is routed to the FPGA						
[PE_RST#]	[JAB1 2]	PCIeRST 18#	JB2 35	B35_L18_N	B1	IO_L18N_T2_AD13N_35
PEX8606 PCIe packet switch						
[on I2C 0] Configuration interface on in I2C0. INTA and FATAL-error are available as test points on JP13						
[REFCLKP]		PCLKP0	JB3 32	MGT_CLK0_N	V9	MGTREFCLK0N_112
[REFCLKN]		PCLKN0	JB3 34	MGT_CLK0_P	U9	MGTREFCLK0P_112
PCIe express reference clocks for PEX switch and Trenz module are regenerated by a SI32202, and are separate outputs of that IC. Its source is either the PCIe clock from the CPU board, or if in HOST most an on-board clock.						
PETP0	-	PE1TXP0	JB3 9	MGT_RX0_P	AA7	MGTRXP0_112
PETN0	-	PE1TXN0	JB3 7	MGT_RX0_N	AB7	MGTRXN0_112
PERP0	-	PE1RXP0	JB3 10	MGT_TX0_P	AA3	MGTTXP0_112
PERN0	-	PE1RXN0	JB3 8	MGT_TX0_N	AB3	MGTTXN0_112
PETP1	-	PE1TXP3	JB3 15	MGT_RX1_P	W8	MGTRXP1_112
PETN1	-	PE1TXN3	JB3 13	MGT_RX1_N	Y8	MGTRXN1_112
PERP1	-	PE1RXP3	JB3 16	MGT_TX1_P	W4	MGTTXP1_112
PERN1	-	PE1RXN3	JB3 14	MGT_TX1_N	Y4	MGTTXN1_112
GPIO8	SEIC 43	LED4	-	-		
GPIO9	SEIC 45	LED3	-	-		
On-board LEDs – not routed off-board						
GPIO10	-	HOST#	JB1 92	MIO9		
HOST# is PCIe host mode (CPU rather than peripheral card configuration) – select by installing JP12						
GPIO11	PCIe/104 CPU_DIR	CPU_DIR	-	-		
CPU_DIR is pulled down on-board. In HOST most, EMC2-DP PCIe lanes are switched for stack-up, so does not need to assert CPU_DIR						
PORTSEL0-3		PORTSEL0-3	-	-		
PORTSEL signals are set via DPI-switch SW2						
PERST#		PCIeSW RST#	-	-		
Switch is reset if PCIe reset or POR is low						
RS232 UARTs						

True RS232 signalling is provided on header RS1 These signals are connected to the FPGA, so can be treated as 3xRS232 UARTs or one UART with control signals						
TX1	RS1 2	RS232_TX1	JB2 21	B34_L2_P	J7	IO_L2P_T0_34
RX1	RS1 3	RS232_RX1	JB2 27	B34_L6_P	M8	IO_L6P_T0_34
TX2	RS1 5	RS232_TX2	JB2 23	B34_L2_N	J6	IO_L2N_T0_34
RX2	RS1 6	RS232_RX2	JB2 31	B35_L16_P	D1	IO_L16P_T2_35
TX3	RS1 8	RS232_TX3	JB2 25	B34_L6_N	M7	IO_L6N_T0_VREF_34
RX3	RS1 9	RS232_RX3	JB2 33	B35_L16_N	C1	IO_L16N_T2_35
LVTTL Inputs						
LVTTL and differential signals are available on JP3.						
TTLP	JP3 2	TTLP	JB2 24	B34_L11_N	K3	IO_L11N_T1_SRCC_34
TTLN	JP3 1	TTLN	JB2 22	B34_L11_P	K4	IO_L11P_T1_SRCC_34
TTLP and N do not have a terminating resistor, unlike the other pairs (TTL0, TTL2) and (TTL1, TTL3).						
TTL0	JP3 5	TTL0	JB2 18	B34_L18_N	P2	IO_L18N_T2_34
TTL1	JP3 7	TTL1	JB2 16	B34_L18_P	P3	IO_L18P_T2_34
TTL2	JP3 6	TTL2	JB2 14	B34_L17_N	R2	IO_L17N_T2_34
TTL3	JP3 8	TTL3	JB2 12	B34_L17_P	R3	IO_L17P_T2_34
100R must not be fitted between TTL0 and TTL2, or TTL1 and TTL3 if they are to be used as single-ended inputs J3 pin 3 is connected to VCCIO34, and pin 4 to ground.						
Misc						
Mode	JP11	MODE	JB1 31	[CPLD] PT7A	CPLD 30	
Jumper to +3.3 or GND To CPLD PT7A/TCK on Trenz module						
LED1	SEIC 46	LED1	JB1 87	B12_L20_P	U19	IO_L20P_T3_13
LED2	SEIC 44	LED2	JB1 99	B12_L22_N	U18	IO_L22N_T3_13
SEIC signals are LEDT1 and LEDT2, derived from the LED signals from the Zynq						
Battery voltage	-	VBAT	JB1 80	-		
VBAT_IN pin on the Trenz module goes to its RTC (ISL12020 – not present on early 7015/7030 modules)						
TrenzRst#	-		JB2 17	-		
Trenz signal RESIN (to module CPLD). Derived on EMC2-DP from reset pushbutton SW1						
PPS1	J5	PPS1	JB2 38	B34_L7_N	K5	IO_L7N_T1_34
Pulse-per-second input						
Unused						
			JB1 27	[CPLD] PT6D	CPLD 32	
EN1 To CPLD PT6D/TDI on Trenz module						
			JB1 29	[CPLD] PT6C	CPLD 1	
PGOOD						

To CPLD PT6C/TDO on Trenz module						
			JB1 44	B12_L2_N	W15	IO_L2N_T0_13
			JB1 79	B12_L21_N	W18	IO_L21N_T3_DQS_13
			JB1 81	B12_L21_P	V18	IO_L21P_T3_DQS_13
			JB1 85	B12_L20_N	V19	IO_L20N_T3_13
			JB1 93	B12_L15_P	AB21	IO_L15P_T2_DQS_13
			JB1 95	B12_L15_N	AB22	IO_L15N_T2_DQS_13

5.2 TE0715 & TE0730 - SEIC Peripherals

Peripheral Pin	Off-board pin	EMC2-DP signal	Carrier Trenz pin	Module signal	FPGA pin	FPGA IO name
HDMI ADV7511						
VSYNC	SEIC 78	HDMI_VSYNC	JB3 60	B34_L13_N	T1	IO_L13N_T2_MRCC_34
HDMI transmitter IC						
HSYNC	SEIC 80	HDMI_HSYNC	JB3 58	B34_L13_P	T2	IO_L13P_T2_MRCC_34
CLK capable						
CLK	SEIC 82	HDMI_CLK	JB3 59	B34_L14_N	U1	IO_L14N_T2_SRCC_34
CLK capable						
DE	SEIC 78	HDMI_DE	JB3 57	B34_L14_P	U2	IO_L14P_T2_SRCC_34
CLK capable						
CEC_CLK	SEIC 75	CEC_CLK	JB2 34	B34_L8_N	J1	IO_L8N_T1_34
SCL	SEIC 79			[I^2C 0 SCL]		
SDA	SEIC 81			[I^2C 0 SDA]		
INT	SEIC 83	HDMI_INT	JB2 26	B34_L12_P	L5	IO_L12P_T1_MRCC_34
CLK capable						
D0	SEIC 88	HDMI_D0	JB3 53	B34_L22_N	M3	IO_L22N_T3_34
D1	SEIC 90	HDMI_D1	JB3 51	B34_L22_P	M4	IO_L22P_T3_34
D2	SEIC 92	HDMI_D2	JB3 49	B34_L10_N	L1	IO_L10N_T1_34
D3	SEIC 94	HDMI_D3	JB3 47	B34_L10_P	L2	IO_L10P_T1_34
D4	SEIC 96	HDMI_D4	JB3 43	B34_L16_N	P1	IO_L16N_T2_34
D5	SEIC 98	HDMI_D5	JB3 44	B34_L21_N	N3	IO_L21N_T3_DQS_34
D6	SEIC 97	HDMI_D6	JB3 41	B34_L16_P	N1	IO_L16P_T2_34
D7	SEIC 95	HDMI_D7	JB3 42	B34_L21_P	N4	IO_L21P_T3_DQS_34
D8	SEIC 93	HDMI_D8	JB3 39	B34_L23_N	R4	IO_L23N_T3_34
D9	SEIC 91	HDMI_D9	JB3 40	B34_L20_N	P5	IO_L20N_T3_34
D10	SEIC 89	HDMI_D10	JB3 37	B34_L23_P	R5	IO_L23P_T3_34
D11	SEIC 87	HDMI_D11	JB3 38	B34_L20_P	P6	IO_L20P_T3_34
SPDIF	SEIC 65	SPDIF_IN	JB2 13	B34_L15_N	M1	IO_L15N_T2_DQS_34
SPDIF from FPGA to ADV7511						
SPDIFOUT	SEIC 67	SPDIF_OUT	JB2 15	B34_L15_P	M2	IO_L15P_T2_DQS_34
SPDIF from ADV7511 to FPGA						
TPD12S016						
LS_OE	SEIC 74	LS_OE	JB2 32	B34_L8_P	J2	IO_L8P_T1_34
HDMI companion IC with I2C level-shifters and protection (ESD and current limit)						
CT_HPD	SEIC 73	CT_HPD	JB2 28	B34_L12_N	L4	IO_L12N_T1_MRCC_34
CLK capable						
Ethernet						

Note: PHY is on the FPGA module						
RJ45 MDI 0 +	SEIC 54	PHY_MDI0_P	JB1 3	-		
RJ45 MDI 0 -	SEIC 56	PHY_MDI0_N	JB1 5	-		
RJ45 MDI 1 +	SEIC 58	PHY_MDI1_P	JB1 9	-		
RJ45 MDI 1 -	SEIC 60	PHY_MDI1_N	JB1 11	-		
RJ45 MDI 2 +	SEIC 59	PHY_MDI2_P	JB1 15	-		
RJ45 MDI 2 -	SEIC 57	PHY_MDI2_N	JB1 17	-		
RJ45 MDI 3 +	SEIC 55	PHY_MDI3_P	JB1 21	-		
RJ45 MDI 3 -	SEIC 53	PHY_MDI3_N	JB1 23	-		
LED 1	SEIC 48	PHY_LED1	JB1 82	B12_L16_P	AB18	IO_L16P_T2_13
LED 2	SEIC 47	PHY_LED2	JB1 84	B12_L16_N	AB19	IO_L16N_T2_13
LEDs on the RJ45 can be driven by the PL (or PS via EMIO).						
PHY → SFP Tx +	SEIC 4	SOUT_P	JB3 4	-		
PHY → SFP Tx -	SEIC 2	SOUT_N	JB3 2	-		
PHY → SFP Rx +	SEIC 3	SIN_P	JB3 3	-		
PHY → SFP Rx -	SEIC 1	SIN_N	JB3 1	-		
EMC2-DP SEIC board does not use these signals from the Ethernet PHY on the module, though they are defined on the connector						
USB OTG						
All of these signals are routed to the USB3320C PHY on the Trenz module						
D+	SEIC 13	OTG_D_P	JB3 48	-		
D-	SEIC 15	OTG_D_N	JB3 50	-		
ID	SEIC 16	OTG_ID	JB3 52	-		
VBUS out enable	SEIC 14	VBUS_V_EN	JB3 54	-		
VBUS	SEIC 12	USB_VBUS	JB3 56	-		
USB UART0						
PS UART0 is exposed via a USB-serial interface on the Micro USB port on the SEIC board						
TX	SEIC 7	UART_TX	JB1 86	MIO15	E17	PS_MIO15_500
RX	SEIC 8	UART_RX	JB1 91	MIO14	B17	PS_MIO14_400
Analogue connectors						
AD0 and AD1 are high-speed SEIC coaxial connectors for external analogue or clock signals.						
AD0P	SEIC 34	AD0P	JB2 58	B35_L1_P	F7	IO_L1P_T0_AD0P_35
AD0N	SEIC 36	AD0N	JB2 56	B35_L1_N	E7	IO_L1N_T0_AD0N_35
AD1P	SEIC 33	AD1P	JB2 64	B35_L3_P	E8	IO_L3P_T0_DQS_AD1P_35
AD1N	SEIC 35	AD1N	JB2 62	B35_L3_N	D8	IO_L3N_T0_DQS_AD1N_35
LEDs						

Corresponding to LEDs on EMC2-DP board
SATA
Optionally routed from EMC2-DP board – described in EMC2-DP section

5.3 TE0715 & TE0730 - EMC2-DP V2 FMC function

Peripheral Pin	Off-board pin	EMC2-DP signal	Carrier Trenz pin	Module signal	FPGA pin	FPGA IO name
FMC						
PRSNT_M2C	FMC H2	PRSNT_M2C_L	JB2 37	B35_L18_P	B2	IO_L18P_T2_AD13P_35
SCL	FMC C30	FMC_SCL	JB1 32	B12_L3_P	W12	IO_L3P_T0_DQS_13
SDA	FMC C31	FMC_SDA	JB1 34	B12_L3_N	W13	IO_L3N_T0_DQS_13
GK0_M2C_P	FMC D4	FMC_TRZ_CK_P	JB3 31	-		
GK0_M2C_N	FMC D5	FMC_TRZ_CK_N	JB3 33	-		
DP0_C2M_P	FMC C2	FMC_TRZ_TX_P	JB3 28	MGT_TX3_P	W2	MGTTXP3_112
DP0_C2M_N	FMC C3	FMC_TRZ_TX_N	JB3 26	MGT_TX3_N	Y2	MGTTXN3_112
DP0_M2C_P	FMC C6	FMC_TRZ_RX_P	JB3 27	MGT_RX3_P	W6	MGTRXP3_112
DP0_M2C_N	FMC C7	FMC_TRZ_RX_N	JB3 25	MGT_RX3_N	Y6	MGTRXN3_112
CK0_M2C_P	FMC H4	FMC_CLK0_P	JB1 60	B12_L12_N	Y15	IO_L12N_T1_MRCC_13
CK0_M2C_N	FMC H5	FMC_CLK0_N	JB1 62	B12_L12_P	Y14	IO_L12P_T1_MRCC_13
CK0_C2M_P	FMC G3	FMC_CLK1_P	JB1 65	B12_L14_N	AA17	IO_L14N_T2_SRCC_13
CK0_C2M_N	FMC G4	FMC_CLK1_N	JB1 67	B12_L14_P	AA16	IO_L14P_T2_SRCC_13
LA00_CC_P	FMC G6	FMC_LA00_P	JB1 76	B12_L13_N	Y19	IO_L3N_T0_DQS_13
LA00_CC_N	FMC G7	FMC_LA00_N	JB1 78	B12_L13_P	Y18	IO_L3P_T0_DQS_13
LA01_CC_P	FMC D8	FMC_LA01_P	JB1 66	B12_L11_N	AA15	IO_L11N_T1_SRCC_13
LA01_CC_N	FMC D9	FMC_LA01_N	JB1 68	B12_L11_P	AA14	IO_L11P_T1_SRCC_13
LA02_P	FMC H7	FMC_LA02_P	JB1 35	B12_L6_P	U13	IO_L6P_T0_13
LA02_N	FMC H8	FMC_LA02_N	JB1 37	B12_L6_N	U14	IO_L6N_T0_13
LA03_P	FMC G9	FMC_LA03_P	JB1 46	B12_L19_P	R17	IO_L19P_T3_13
LA03_N	FMC G10	FMC_LA03_N	JB1 48	B12_L19_N	T17	IO_L19N_T3_VREF_13
LA04_P	FMC H10	FMC_LA04_P	JB1 50	B12_L1_P	V13	IO_L1P_T0_13
LA04_N	FMC H11	FMC_LA04_N	JB1 52	B12_L1_N	V14	IO_L1N_T0_13
LA05_P	FMC D11	FMC_LA05_P	JB1 49	B12_L8_P	AA12	IO_L8P_T1_13
LA05_N	FMC D12	FMC_LA05_N	JB1 51	B12_L8_N	AB12	IO_L8N_T1_13
LA06_P	FMC C10	FMC_LA06_P	JB1 45	B12_L7_P	AA11	IO_L7P_T1_13
LA06_N	FMC C11	FMC_LA06_N	JB1 47	B12_L7_N	AB11	IO_L7N_T1_13
LA07_P	FMC H13	FMC_LA07_P	JB1 55	B12_L10_P	Y12	IO_L10P_T1_13
LA07_N	FMC H14	FMC_LA07_N	JB1 57	B12_L10_N	Y13	IO_L10N_T1_13
LA08_P	FMC G12	FMC_LA08_P	JB1 56	B12_L9_P	AB13	IO_L9P_T1_DQS_13
LA08_N	FMC G13	FMC_LA08_N	JB1 58	B12_L9_N	AB14	IO_L9N_T1_DQS_13
LA09_P	FMC D14	FMC_LA09_P	JB2 42	B35_L21_N	E3	IO_L21N_T3_DQS_AD14N_35
LA09_N	FMC D15	FMC_LA09_N	JB2 44	B35_L21_P	E4	IO_L21P_T3_DQS_AD14P_35
LA10_P	FMC C14	FMC_LA10_P	JB1 59	B12_L23_P	V16	IO_L23P_T3_13
LA10_N	FMC C15	FMC_LA10_N	JB1 61	B12_L23_N	W16	IO_L23N_T3_13
LA11_P	FMC H16	FMC_LA11_P	JB1 39	B12_L4_P	V11	IO_L4P_T0_13
LA11_N	FMC H17	FMC_LA11_N	JB1 41	B12_L4_N	W11	IO_L4N_T0_13
LA12_P	FMC G15	FMC_LA12_P	JB1 36	B12_L5_P	U11	IO_L5P_T0_13
LA12_N	FMC G16	FMC_LA12_N	JB1 38	B12_L5_N	U12	IO_L5N_T0_13

LA13_P	FMC D17	FMC_LA13_P	JB1 70	B12_L17_P	AB16	IO_L11P_T1_SRCC_13
LA13_N	FMC D18	FMC_LA13_N	JB1 72	B12_L17_N	AB17	IO_L11N_T1_SRCC_13
LA14_P	FMC C18	FMC_LA14_P	JB1 69	B12_L24_N	Y17	IO_L24N_T3_13
LA14_N	FMC C19	FMC_LA14_N	JB1 71	B12_L24_P	W17	IO_L24P_T3_13
LA15_P	FMC H19	FMC_LA15_P	JB1 75	B12_L18_P	AA19	IO_L18P_T2_13
LA15_N	FMC H20	FMC_LA15_N	JB1 77	B12_L18_N	AA20	IO_L18N_T2_13
LA16_P	FMC G18	FMC_LA16_P	JB2 74	B35_L4_P	G8	IO_L4P_T0_35
LA16_N	FMC G19	FMC_LA16_N	JB2 72	B35_L4_N	G7	IO_L4N_T0_35
LA17_CC_P	FMC D20	FMC_LA17_P	JB2 55	B35_L12_P	D5	IO_L12P_T1_MRCC_35
LA17_CC_N	FMC D21	FMC_LA17_N	JB2 57	B35_L12_N	C4	IO_L12N_T1_MRCC_35
LA18_CC_P	FMC C22	FMC_LA18_P	JB2 52	B35_L11_P	C6	IO_L11P_T1_SRCC_35
LA18_CC_N	FMC C23	FMC_LA18_N	JB2 54	B35_L11_N	C5	IO_L11N_T1_SRCC_35
LA19_P	FMC H22	FMC_LA19_P	JB2 51	B35_L14_P	D3	IO_L14P_T2_AD4P_SRCC_35
LA19_N	FMC H23	FMC_LA19_N	JB2 53	B35_L14_N	C3	IO_L14N_T2_AD4N_SRCC_35
LA20_P	FMC G21	FMC_LA20_P	JB2 48	B35_L8_P	B7	IO_L8P_T1_AD10P_35
LA20_N	FMC G22	FMC_LA20_N	JB2 46	B35_L8_N	B6	IO_L8N_T1_AD10N_35
LA21_P	FMC H25	FMC_LA21_P	JB2 65	B35_L2_N	D6	IO_L2N_T0_AD8N_35
LA21_N	FMC H26	FMC_LA21_N	JB2 67	B35_L2_P	D7	IO_L2P_T0_AD8P_35
LA22_P	FMC G24	FMC_LA22_P	JB2 61	B35_L23_N	F1	IO_L23N_T3_35
LA22_N	FMC G25	FMC_LA22_N	JB2 63	B35_L23_P	F2	IO_L23P_T3_35
LA23_P	FMC D23	FMC_LA23_P	JB2 71	B35_L17_P	E2	IO_L17P_T2_AD5P_35
LA23_N	FMC D24	FMC_LA23_N	JB2 73	B35_L17_N	D2	IO_L17N_T2_AD5N_35
LA24_P	FMC H28	FMC_LA24_P	JB2 82	B35_L5_N	E5	IO_L5N_T0_AD9N_35
LA24_N	FMC H29	FMC_LA24_N	JB2 84	B35_L5_P	F5	IO_L5P_T0_AD9P_35
LA25_P	FMC G27	FMC_LA25_P	JB2 75	B35_L24_P	H1	IO_L24P_T3_AD15P_35
LA25_N	FMC G28	FMC_LA25_N	JB2 77	B35_L24_N	G1	IO_L24N_T3_AD15N_35
LA26_P	FMC D26	FMC_LA26_P	JB2 66	B35_L7_P	C8	IO_L7P_T1_AD2P_35
LA26_N	FMC D27	FMC_LA26_N	JB2 68	B35_L7_N	B8	IO_L7N_T1_AD2N_35
LA27_P	FMC C26	FMC_LA27_P	JB2 76	B35_L19_N	H3	IO_L19N_T3_VREF_35
LA27_N	FMC C27	FMC_LA27_N	JB2 78	B35_L19_P	H4	IO_L19P_T3_35
LA28_P	FMC H31	FMC_LA28_P	JB2 86	B35_L6_N	F6	IO_L6N_T0_VREF_35
LA28_N	FMC H32	FMC_LA28_N	JB2 88	B35_L6_P	G6	IO_L6P_T0_35
LA29_P	FMC G30	FMC_LA29_P	JB2 81	B35_L9_N	A6	IO_L9N_T1_DQS_AD3N_35
LA29_N	FMC G31	FMC_LA29_N	JB2 83	B35_L9_P	A7	IO_L9P_T1_DQS_AD3P_35
LA30_P	FMC H34	FMC_LA30_P	JB2 91	B25_L10_N	A4	IO_L10N_T1_AD11N_35
LA30_N	FMC H35	FMC_LA30_N	JB2 93	B35_L10_P	A5	IO_L10P_T1_AD11P_35
LA31_P	FMC G33	FMC_LA31_P	JB2 85	B35_L22_N	G2	IO_L22N_T3_AD7N_35
LA31_N	FMC G34	FMC_LA31_N	JB2 87	B35_L22_P	G3	IO_L22P_T3_AD7P_35
LA32_P	FMC H37	FMC_LA32_P	JB2 99	B35_L25	H5	IO_L25_VRP_35
LA32_N	FMC H38	FMC_LA32_N	JB2 90	B35_L0	H6	IO_0_VRN_35
LA33_P	FMC G36	FMC_LA33_P	JB2 95	B35_L20_N	F4	IO_L20N_T3_AD6N_35
LA33_N	FMC G37	FMC_LA33_N	JB2 97	B35_L20_P	G4	IO_L20P_T3_AD6P_35

6 TE0712 EMC-DP and SEIC

6.1 TE0712 - EMC2-DP Peripherals

Peripheral Pin	Off-board pin	EMC2-DP signal	Carrier Trenz pin	Module signal	FPGA pin	FPGA IO name
MicroSD						
CLK	-	SD_CLK	JB1 28	B13_L9_P	AA10	IO_L9P_T1_DQS_13
CMD	-	SD_CMD	JB1 26	B13_L9_N	AA11	IO_L9N_T1_DQS_13
D0	-	SD_D0	JB1 24	B13_L11_P	Y11	IO_L11P_T1_SRCC_13
D1	-	SD_D1	JB1 22	B13_L11_N	Y12	IO_L11N_T1_SRCC_13
D2	-	SD_D2	JB1 20	B13_L3_N	AB13	IO_L3N_T0_DQS_13
D3	-	SD_D3	JB1 18	B13_L3_P	AA13	IO_L3P_T0_DQS_13
Card present sw	-	SD_SW	JB1 42	B16_L23_P	E21	IO_L23P_T3_16
DS2432 SHA NVM + ID						
DS2432 is a Dallas 1-wire protected NVM with SHA-1 engine and 1kbit storage. Connected via a MAX3394 level translator						
1-WIRE	-	WIRE1	JB2 36	B14_L15_P	AA19	IO_L15P_T2_DQS_RDWR_B_14
NVM + MAC						
[on I2C 0]						
DS1337 RTC						
[on I2C 0]						
nINTA		RTC_INT#	JB1 88	B14_L18_P	U17	IO_L18P_T2_A12_D28_14
Clock Synthesiser – SI5338A						
[on I2C 0] Configured via I2C0 J6 is connected to IN6 of the SI5338 25MHz crystal connected to IN1/IN2						
CLK0A	-	CLK1	JB2 47	B15_L13_N	K19	IO_L13N_T2_MRCC_15
CLK capable; J6 is connected to IN6 of the SI5338						
CLK1A	-	CLK2	JB2 45	B15_L13_P	K18	IO_L13P_T2_MRCC_15
CLK capable						
CLK2A	-	CLK3	JB2 43	B15_L7_P	J22	IO_L7P_T1_AD2P_15
NOT a clock capable pin, but can be used with set_property CLOCK_DEDICATED_ROUTE FALSE						
CLK3A	-	CLK4	JB2 41	B15_L7_N	H22	IO_L7N_T1_AD2N_15
NOT a clock capable pin						
IN1	-	-	-	-		
IN2	-	-	-	-		
IN3	J6	unnamed	-	-		
I2C [0]						
SCL	-	I2C0_SCL	JB1 96	B14_L4_P	T21	IO_L4P_T0_D04_14

SI5338A clock synthesizer, DS1337 RTC, 24AA02E64 MAC address + NVM, MPU-9150 motion tracking device, PEX8606 PCIe switch						
SDA	-	I2C0_SDA	JB1 94	B14_L9_N	Y22	IO_L9N_T1_DQS_D13_14
I2C [1]						
SCL	-	I2C1_SCL	JB1 100	B14_L24_N	R17	IO_L24N_T3_A00_D16_14
PCIe SMB						
SDA	-	I2C1_SDA	JB1 98	B14_L4_N	U21	IO_L4N_T0_D05_14
SATA						
TX_P	[SEIC 23]	SATA_TRZ_TX_P	JB3 22	MGT_TX2_P	B6	MGTPTXP2_216
TX_N	[SEIC 21]	SATA_TRZ_TX_N	JB3 20	MGT_TX2_N	A6	MGTPTXN2_216
RX_P	[SEIC 24]	SATA_TRZ_RX_P	JB3 21	MGT_RX2_P	B10	MGTPRXP2_216
RX_N	[SEIC 22]	SATA_TRZ_RX_N	JB3 19	MGT_RX2_N	A10	MGTPRXN2_216
PCIe Reset						
Level-shifted, this PCIe reset signal from the stack-down connector is routed to the FPGA						
[PE_RST#]	[JAB1 2]	PCIeRST 18#	JB2 35	B15_L8_N	G20	IO_L8N_T1_AD10N_15
PEX8606 PCIe packet switch						
[on I2C 0] Configuration interface on in I2C0. INTA and FATAL-error are available as test points on JP13						
[REFCLKP]		PCLKP0	JB3 32	MGT_CLK1_N	E10	MGTREFCLK1N_216
[REFCLKN]		PCLKN0	JB3 34	MGT_CLK1_P	F10	MGTREFCLK1P_216
PCIe express reference clocks for PEX switch and Trenz module are regenerated by a SI32202, and are separate outputs of that IC. Its source is either the PCIe clock from the CPU board, or if in HOST most an on-board clock.						
PETP0	-	PE1TXP0	JB3 9	MGT_RX0_P	B8	MGTPRXP0_216
PETN0	-	PE1TXN0	JB3 7	MGT_RX0_N	A8	MGTPRXN0_216
PERP0	-	PE1RXP0	JB3 10	MGT_TX0_P	B4	MGTPTXP0_216
PERN0	-	PE1RXN0	JB3 8	MGT_TX0_N	A4	MGTPTXN0_216
PETP1	-	PE1TXP3	JB3 15	MGT_RX1_P	D11	MGTPRXP1_216
PETN1	-	PE1TXN3	JB3 13	MGT_RX1_N	C11	MGTPRXN1_216
PERP1	-	PE1RXP3	JB3 16	MGT_TX1_P	D5	MGTPTXP1_216
PERN1	-	PE1RXN3	JB3 14	MGT_TX1_N	C5	MGTPTXN1_216
GPIO8	SEIC 43	LED4	-	-		
GPIO9	SEIC 45	LED3	-	-		
On-board LEDs – not routed off-board						
GPIO10	-	HOST#	JB1 92	B14_L9_P	Y21	IO_L9P_T1_DQS_14
HOST# is PCIe host mode (CPU rather than peripheral card configuration) – select by installing JP12						
GPIO11	PCIe/104 CPU_DIR	CPU_DIR	-	-		
CPU_DIR is pulled down on-board. In HOST most, EMC2-DP PCIe lanes are switched for stack-up, so does not need to assert CPU_DIR						

PORTSEL0-3		PORTSEL0-3	-	-		
PORTSEL signals are set via DPI-switch SW2						
PERST#		PCIeSW RST#	-	-		
Switch is reset if PCIe reset or POR is low						
RS232 UARTs						
True RS232 signalling is provided on header RS1 These signals are connected to the FPGA, so can be treated as 3xRS232 UARTs or one UART with control signals						
TX1	RS1 2	RS232_TX1	JB2 21	B14_L12_P	W19	IO_L12P_T1_MRCC_14
CLK capable						
RX1	RS1 3	RS232_RX1	JB2 27	B14_L11_N	V20	IO_L11N_T1_SRCC_14
CLK capable						
TX2	RS1 5	RS232_TX2	JB2 23	B14_L12_N	W20	IO_L12N_T1_MRCC_14
CLK capable						
RX2	RS1 6	RS232_RX2	JB2 31	B15_L9_N	K22	IO_L9N_T1_DQS_AD3N_15
TX3	RS1 8	RS232_TX3	JB2 25	B14_L11_P	U20	IO_L11P_T1_SRCC_14
CLK capable						
RX3	RS1 9	RS232_RX3	JB2 33	B15_L9_P	K21	IO_L9P_T1_DQS_AD3P_15
LVTTL Inputs						
LVTTL and differential signals are available on JP3.						
TTLP	JP3 2	TTLP	JB2 24	B14_L14_N	V19	IO_L14N_T2_SRCC_14
TTLN	JP3 1	TTLN	JB2 22	B14_L14_P	V18	IO_L14P_T2_SRCC_14
TTLP and N do not have a terminating resistor, unlike the other pairs (TTL0, TTL2) and (TTL1, TTL3). They are CLK Capable						
TTL0	JP3 5	TTL0	JB2 18	B14_L17_P	AA18	IO_L17P_T2_A14_D30_14
TTL1	JP3 7	TTL1	JB2 16	B14_L17_N	AB18	IO_L17N_T2_A13_D29_14
TTL2	JP3 6	TTL2	JB2 14	B14_L8_P	AA20	IO_L8P_T1_D11_14
TTL3	JP3 8	TTL3	JB2 12	B14_L8_N	AA21	IO_L8N_T1_D12_14
100R must not be fitted between TTL0 and TTL2, or TTL1 and TTL3 if they are to be used as single-ended inputs J3 pin 3 is connected to VCCIO34, and pin 4 to ground.						
Misc						
Mode	JP11	MODE	JB1 31	[CPLD] PB4C	CPLD 13	
Jumper to +3.3 or GND To CPLD PB4C on Trenz module						
LED1	SEIC 46	LED1	JB1 87	B16_L6_P	D14	IO_L6P_T0_16
LED2	SEIC 44	LED2	JB1 99	B16_L1_P	F13	IO_L1P_T0_16
SEIC signals are LEDT1 and LEDT2, derived from the LED signals from the module						
Battery voltage	-	VBAT	JB1 80	-		
N/C on TE0712						
TrenzRst#	-		JB2 17	-		

Trenz signal RESIN (to module CPLD). Derived on EMC2-DP from reset pushbutton SW1						
PPS1	J5	PPS1	JB2 38	B14_L15_N	AB20	IO_L15N_T2_DQS_DOUT_CSO_B_14
Pulse-per-second input						
Unused						
			JB1 27	[CPLD] PB4A	CPLD 11	
EN1 To CPLD PB4A/PCLKT2_0 on Trenz module						
			JB1 29	[CPLD] PB4B	CPLD 12	
PGOOD To CPLD PB4B/PCLKC2_0 on Trenz module						
			JB1 44	B16_L23_N	D21	IO_L23N_T3_16
			JB1 79	B16_L2_N	E17	IO_L2N_T0_16
			JB1 81	B16_L2_P	F16	IO_L2P_T0_16
			JB1 85	B16_L6_N	D15	IO_L6N_T0_VREF_16
			JB1 93	B16_L4_N	E14	IO_L4N_T0_16
			JB1 95	B16_L4_P	E13	IO_L4P_T0_16

6.2 TE0712 - SEIC Peripherals

Peripheral Pin	Off-board pin	EMC2-DP signal	Carrier Trenz pin	Module signal	FPGA pin	FPGA IO name
HDMI ADV7511						
VSYNC	SEIC 78	HDMI_VSYNC	JB3 60	B13_L13_N	V14	IO_L13N_T2_MRCC_13
HDMI transmitter IC						
HSYNC	SEIC 80	HDMI_HSYNC	JB3 58	B13_L13_P	V13	IO_L13P_T2_MRCC_13
CLK	SEIC 82	HDMI_CLK	JB3 59	B13_L12_N	W12	IO_L12N_T1_MRCC_13
CLK capable						
DE	SEIC 78	HDMI_DE	JB3 57	B13_L12_P	W11	IO_L12P_T1_MRCC_13
CLK capable						
CEC_CLK	SEIC 75	CEC_CLK	JB2 34	B14_L16_N	W17	IO_L16N_T2_A15_D31_14
SCL	SEIC 79			[I^2C 0 SCL]		
SDA	SEIC 81			[I^2C 0 SDA]		
INT	SEIC 83	HDMI_INT	JB2 26	B14_L13_P	Y18	IO_L13P_T2_MRCC_14
CLK capable						
D0	SEIC 88	HDMI_D0	JB3 53	B13_L2_P	AB16	IO_L2P_T0_13
D1	SEIC 90	HDMI_D1	JB3 51	B13_L2_N	AB17	IO_L2N_T0_13
D2	SEIC 92	HDMI_D2	JB3 49	B13_L4_N	AB15	IO_L4N_T0_13
D3	SEIC 94	HDMI_D3	JB3 47	B13_L4_P	AA15	IO_L4P_T0_13
D4	SEIC 96	HDMI_D4	JB3 43	B13_L1_N	AA16	IO_L1N_T0_13
D5	SEIC 98	HDMI_D5	JB3 44	B13_L15_N	T15	IO_L15N_T2_DQS_13
D6	SEIC 97	HDMI_D6	JB3 41	B13_L1_P	Y16	IO_L1P_T0_13
D7	SEIC 95	HDMI_D7	JB3 42	B13_L15_P	T14	IO_L15P_T2_DQS_13
D8	SEIC 93	HDMI_D8	JB3 39	B13_L16_N	W16	IO_L16N_T2_13
D9	SEIC 91	HDMI_D9	JB3 40	B13_L10_N	W10	IO_L10N_T1_13
D10	SEIC 89	HDMI_D10	JB3 37	B13_L16_P	W15	IO_L16P_T2_13
D11	SEIC 87	HDMI_D11	JB3 38	B13_L10_P	V10	IO_L10P_T1_13
SPDIF	SEIC 65	SPDIF_IN	JB2 13	B14_L10_N	AB22	IO_L10N_T1_D15_14
SPDIF from FPGA to ADV7511						
SPDIFOUT	SEIC 67	SPDIF_OUT	JB2 15	B14_L10_P	AB21	IO_L10P_T1_D14_14
SPDIF from ADV7511 to FPGA						
TPD12S016						
LS_OE	SEIC 74	LS_OE	JB2 32	B14_L16_P	V17	IO_L16P_T2_CSI_B_14
HDMI companion IC with I2C level-shifters and protection (ESD and current limit)						
CT_HPD	SEIC 73	CT_HPD	JB2 28	B14_L13_N	Y19	IO_L13N_T2_MRCC_14
CLK capable						
Ethernet						
Note: PHY is on the FPGA module						

RJ45 MDI 0 +	SEIC 54	PHY_MDI0_P	JB1 3	ETH_TD_P		
RJ45 MDI 0 -	SEIC 56	PHY_MDI0_N	JB1 5	ETH_TD_N		
RJ45 MDI 1 +	SEIC 58	PHY_MDI1_P	JB1 9	ETH_RD_P		
RJ45 MDI 1 -	SEIC 60	PHY_MDI1_N	JB1 11	ETH_RD_N		
RJ45 MDI 2 +	SEIC 59	PHY_MDI2_P	JB1 15	B13_L6_N	Y14	IO_L6N_T0_VREF_13
RJ45 MDI 2 -	SEIC 57	PHY_MDI2_N	JB1 17	B13_L6_P	W14	IO_L6P_T0_13
RJ45 MDI 3 +	SEIC 55	PHY_MDI3_P	JB1 21	B13_L5_N	AA14	IO_L5N_T0_13
RJ45 MDI 3 -	SEIC 53	PHY_MDI3_N	JB1 23	B13_L5_P	Y13	IO_L5P_T0_13
LED 1	SEIC 48	PHY_LED1	JB1 82	B16_L8_N	B13	IO_L8N_T1_16
LED 2	SEIC 47	PHY_LED2	JB1 84	B16_L8_P	C13	IO_L8P_T1_16
LEDs on the RJ45 can be driven by the PL						
PHY → SFP Tx +	SEIC 4	SOUT_P	JB3 4	B13_L17_N	U16	IO_L17N_T2_13
PHY → SFP Tx -	SEIC 2	SOUT_N	JB3 2	B13_L17_P	T16	IO_L17P_T2_13
PHY → SFP Rx +	SEIC 3	SIN_P	JB3 3	B13_L14_N	V15	IO_L14N_T2_SRCC_13
PHY → SFP Rx -	SEIC 1	SIN_N	JB3 1	B13_L14_P	U15	IO_L14P_T2_SRCC_13
Present EMC2-DP SEIC does not make use of these signals.						
USB OTG						
The TE0712 module does not have a USB PHY						
D+	SEIC 13	OTG_D_P	JB3 48	B14_L5_P	P19	IO_L5P_T0_D06_14
D-	SEIC 15	OTG_D_N	JB3 50	B14_L5_N	R19	IO_L5N_T0_D07_14
ID	SEIC 16	OTG_ID	JB3 52	B14_L20_P	R18	IO_L20P_T3_A08_D24_14
VBUS out enable	SEIC 14	VBUS_V_EN	JB3 54	B14_L20_N	T18	IO_L20N_T3_A07_D23_14
VBUS	SEIC 12	USB_VBUS	JB3 56	-		
N/C on TE0712						
USB UART0						
PS UART0 is exposed via a USB-serial interface on the Micro USB port on the SEIC board						
TX	SEIC 7	UART_TX	JB1 86	B14_L18_N	U18	IO_L18N_T2_A11_D27_14
RX	SEIC 8	UART_RX	JB1 91	B14_L24_P	P16	IO_L24P_T3_A01_D17_14
Analogue connectors						
AD0 and AD1 are high-speed SEIC coaxial connectors for external analogue or clock signals. The EMC2 board signals are appropriate to the Zynq modules but not TE0712						
AD0P	SEIC 34	AD0P	JB2 58	B15_L3_N	H14	IO_L3N_T0_DQS_AD1N_15
AD0N	SEIC 36	AD0N	JB2 56	B15_L3_P	J14	IO_L3P_T0_DQS_AD1P_15
AD1P	SEIC 33	AD1P	JB2 64	B15_L17_P	N18	IO_L17P_T2_A16_15
AD1N	SEIC 35	AD1N	JB2 62	B15_L17_N	N19	IO_L17N_T2_A15_15
LEDs						
Corresponding to LEDs on EMC2-DP board						

SATA
Optionally routed from EMC2-DP board – described in EMC2-DP section

6.3 TE0712 - EMC2-DP V2 FMC function

Peripheral Pin	Off-board pin	EMC2-DP signal	Carrier Trenz pin	Module signal	FPGA pin	FPGA IO name
FMC						
PRSNT_M2C	FMC H2	PRSNT_M2C_L	JB2 37	B15_L8_P	H20	IO_L8P_T1_AD10P_15
SCL	FMC C30	FMC_SCL	JB1 32	B16_L22_P	E22	IO_L22P_T3_16
SDA	FMC C31	FMC_SDA	JB1 34	B16_L22_N	D22	IO_L22N_T3_16
GK0_M2C_P	FMC D4	FMC_TRZ_CK_P	JB3 31	-		
GK0_M2C_N	FMC D5	FMC_TRZ_CK_N	JB3 33	-		
DP0_C2M_P	FMC C2	FMC_TRZ_TX_P	JB3 28	MGT_TX3_P	D7	MGTPTXP3_216
DP0_C2M_N	FMC C3	FMC_TRZ_TX_N	JB3 26	MGT_TX3_N	C7	MGTPTXN3_216
DP0_M2C_P	FMC C6	FMC_TRZ_RX_P	JB3 27	MGT_RX3_P	D9	MGTPRXP3_216
DP0_M2C_N	FMC C7	FMC_TRZ_RX_N	JB3 25	MGT_RX3_N	C9	MGTPRXN3_216
CK0_M2C_P	FMC H4	FMC_CLK0_P	JB1 60	B16_L13_P	C18	IO_L13P_T2_MRCC_16
CK0_M2C_N	FMC H5	FMC_CLK0_N	JB1 62	B16_L13_N	C19	IO_L13N_T2_MRCC_16
CK0_C2M_P	FMC G2	FMC_CLK1_P	JB1 65	B16_L11_P	B17	IO_L11P_T1_SRCC_16
CK0_C2M_N	FMC G3	FMC_CLK1_N	JB1 67	B16_L11_N	B18	IO_L11N_T1_SRCC_16
LA00_CC_P	FMC G6	FMC_LA00_P	JB1 76	B16_L12_P	D17	IO_L12P_T1_MRCC_16
LA00_CC_N	FMC G7	FMC_LA00_N	JB1 78	B16_L12_N	C17	IO_L12N_T1_MRCC_16
LA01_CC_P	FMC D8	FMC_LA01_P	JB1 66	B16_L14_P	E19	IO_L14P_T2_SRCC_16
LA01_CC_N	FMC D9	FMC_LA01_N	JB1 68	B16_L14_N	D19	IO_L14N_T2_SRCC_16
LA02_P	FMC H7	FMC_LA02_P	JB1 35	B16_L16_P	B20	IO_L16P_T2_16
LA02_N	FMC H8	FMC_LA02_N	JB1 37	B16_L16_N	A20	IO_L16N_T2_16
LA03_P	FMC G9	FMC_LA03_P	JB1 46	B16_L15_P	F18	IO_L15P_T2_DQS_16
LA03_N	FMC G10	FMC_LA03_N	JB1 48	B16_L15_N	E18	IO_L15N_T2_DQS_16
LA04_P	FMC H10	FMC_LA04_P	JB1 50	B16_L20_P	C22	IO_L20P_T3_16
LA04_N	FMC H11	FMC_LA04_N	JB1 52	B16_L20_N	B22	IO_L20N_T3_16
LA05_P	FMC D11	FMC_LA05_P	JB1 49	B16_L18_N	F20	IO_L18N_T2_16
LA05_N	FMC D12	FMC_LA05_N	JB1 51	B16_L18_P	F19	IO_L18P_T2_16
LA06_P	FMC C10	FMC_LA06_P	JB1 45	B16_L17_N	A19	IO_L17N_T2_16
LA06_N	FMC C11	FMC_LA06_N	JB1 47	B16_L17_P	A18	IO_L17P_T2_16
LA07_P	FMC H13	FMC_LA07_P	JB1 55	B16_L9_N	A16	IO_L9N_T1_DQS_16
LA07_N	FMC H14	FMC_LA07_N	JB1 57	B16_L9_P	A15	IO_L9P_T1_DQS_16
LA08_P	FMC G12	FMC_LA08_P	JB1 56	B16_L21_P	B21	IO_L21P_T3_DQS_16
LA08_N	FMC G13	FMC_LA08_N	JB1 58	B16_L21_N	A21	IO_L21N_T3_DQS_16
LA09_P	FMC D14	FMC_LA09_P	JB2 42	B15_L23_P	L16	IO_L23P_T3_FOE_B_15
LA09_N	FMC D15	FMC_LA09_N	JB2 44	B15_L23_N	K16	IO_L23N_T3_FWE_B_15
LA10_P	FMC C14	FMC_LA10_P	JB1 59	B16_L7_N	B16	IO_L7N_T1_16
LA10_N	FMC C15	FMC_LA10_N	JB1 61	B16_L7_P	B15	IO_L7P_T1_16
LA11_P	FMC H16	FMC_LA11_P	JB1 39	B16_L19_N	C20	IO_L19N_T3_VREF_16

LA11_N	FMC H17	FMC_LA11_N	JB1 41	B16_L19_P	D20	IO_L19P_T3_16
LA12_P	FMC G15	FMC_LA12_P	JB1 36	B16_L24_N	G21	IO_L24N_T3_16
LA12_N	FMC G16	FMC_LA12_N	JB1 38	B16_L24_P	G22	IO_L24P_T3_16
LA13_P	FMC D17	FMC_LA13_P	JB1 70	B16_L3_N	C15	IO_L3N_T0_DQS_16
LA13_N	FMC D18	FMC_LA13_N	JB1 72	B16_L3_P	C14	IO_L3P_T0_DQS_16
LA14_P	FMC C18	FMC_LA14_P	JB1 69	B16_L10_N	A14	IO_L10N_T1_16
LA14_N	FMC C19	FMC_LA14_N	JB1 71	B16_L10_P	A13	IO_L10P_T1_16
LA15_P	FMC H19	FMC_LA15_P	JB1 75	B16_L5_N	D16	IO_L5N_T0_16
LA15_N	FMC H20	FMC_LA15_N	JB1 77	B16_L5_P	E16	IO_L5P_T0_16
LA16_P	FMC G18	FMC_LA16_P	JB2 74	B15_L1_N	G13	IO_L1N_T0_AD0N_15
LA16_N	FMC G19	FMC_LA16_N	JB2 72	B15_L1_P	H13	IO_L1P_T0_AD0P_15
LA17_CC_P	FMC D20	FMC_LA17_P	JB2 55	B15_L12_P	J19	IO_L12P_T1_MRCC_15
LA17_CC_N	FMC D21	FMC_LA17_N	JB2 57	B15_L12_N	H19	IO_L12N_T1_MRCC_15
LA18_CC_P	FMC C22	FMC_LA18_P	JB2 52	B15_L11_P	J20	IO_L11P_T1_SRCC_15
LA18_CC_N	FMC C23	FMC_LA18_N	JB2 54	B15_L11_N	J21	IO_L11N_T1_SRCC_15
LA19_P	FMC H22	FMC_LA19_P	JB2 51	B15_L14_P	L19	IO_L14P_T2_SRCC_15
LA19_N	FMC H23	FMC_LA19_N	JB2 53	B15_L14_N	L20	IO_L14N_T2_SRCC_15
LA20_P	FMC G21	FMC_LA20_P	JB2 48	B15_L19_N	K14	IO_L19N_T3_A21_VREF_15
LA20_N	FMC G22	FMC_LA20_N	JB2 46	B15_L19_P	K13	IO_L19P_T2_T3_A22_15
LA21_P	FMC H25	FMC_LA21_P	JB2 65	B15_L18_P	N20	IO_L18P_T2_A24_15
LA21_N	FMC H26	FMC_LA21_N	JB2 67	B15_L18_N	M20	IO_L18N_T2_A23_15
LA22_P	FMC G24	FMC_LA22_P	JB2 61	B15_L10_N	L21	IO_L10N_T1_AD11N_15
LA22_N	FMC G25	FMC_LA22_N	JB2 63	B15_L10_P	M21	IO_L10P_T1_AD11P_15
LA23_P	FMC D23	FMC_LA23_P	JB2 71	B15_L20_P	M13	IO_L20P_T3_A20_15
LA23_N	FMC D24	FMC_LA23_N	JB2 73	B15_L20_N	L13	IO_L20N_T3_A19_15
LA24_P	FMC H28	FMC_LA24_P	JB2 82	B15_L4_P	G17	IO_L4P_T0_15
LA24_N	FMC H29	FMC_LA24_N	JB2 84	B15_L4_N	G18	IO_L4N_T0_15
LA25_P	FMC G27	FMC_LA25_P	JB2 75	B15_L15_P	N22	IO_L15P_T2_DQS_15
LA25_N	FMC G28	FMC_LA25_N	JB2 77	B15_L15_N	M22	IO_L15N_T2_DSQ_ADV_B_15
LA26_P	FMC D26	FMC_LA26_P	JB2 66	B15_L16_P	M18	IO_L16P_T2_A28_15
LA26_N	FMC D27	FMC_LA26_N	JB2 68	B15_L16_N	L18	IO_L16N_T2_A27_15
LA27_P	FMC C26	FMC_LA27_P	JB2 76	B15_L2_P	G15	IO_L2P_T0_AD8P_15
LA27_N	FMC C27	FMC_LA27_N	JB2 78	B15_L2_N	G16	IO_L2N_T0_AD8N_15
LA28_P	FMC H31	FMC_LA28_P	JB2 86	B15_L5_N	H15	IO_L5N_T0_AD9N_15
LA28_N	FMC H32	FMC_LA28_N	JB2 88	B15_L5_P	J15	IO_L5P_T0_AD9P_15
LA29_P	FMC G30	FMC_LA29_P	JB2 81	B15_L6_N	H18	IO_L6N_T0_VREF_15
LA29_N	FMC G31	FMC_LA29_N	JB2 83	B15_L6_P	H17	IO_L6P_T0_15
LA30_P	FMC H34	FMC_LA30_P	JB2 91	B15_L24_N	M16	IO_L24N_T3_RS0_15
LA30_N	FMC H35	FMC_LA30_N	JB2 93	B15_L24_P	M15	IO_L24P_T3_RS1_15

LA31_P	FMC G33	FMC_LA31_P	JB2 85	B15_L21_P	K17	IO_L21P_T3_DQS_15
LA31_N	FMC G34	FMC_LA31_N	JB2 87	B15_L21_N	J17	IO_L21N_T3_DQS_A18_15
LA32_P	FMC H37	FMC_LA32_P	JB2 99	B15_IO25	M17	IO_25_15
LA32_N	FMC H38	FMC_LA32_N	JB2 90	B15_IO0	J16	IO_0_15
LA33_P	FMC G36	FMC_LA33_P	JB2 95	B15_L22_N	L15	IO_L22N_T3_A16_15
LA33_N	FMC G37	FMC_LA33_N	JB2 97	B15_L22_P	L14	IO_L22P_T3_A17_15

7 Trenz master pinout

TE0712		TE0715		JMx	Jxx	JBx	EMC2-DP V2		Sort Order
FPGA PIN	Signal Name	FPGA PIN	Signal Name						
-	**VIN_DCDC**	-	**VIN_DCDC**	1	Jx1	2	**5.0V**		0.5
-	**VIN_DCDC**	-	**VIN_DCDC**	3	Jx1	4	**5.0V**		1.5
-	**VIN_DCDC**	-	**VIN_DCDC**	5	Jx1	6	**5.0V**		2.5
-	NOSEQ	-	NOSEQ	7	Jx1	8			3.5
-	**VCCIO_B16_IN**	-	**VCCIO_B13_IN**	9	Jx1	10	**VCCIO35**	JP8	4.5
-	**VCCIO_B16_IN**	-	**VCCIO_B13_IN**	11	Jx1	12	**VCCIO35**	JP8	5.5
-	**VIN_3.3**	-	**VIN_3.3**	13	Jx1	14	**3.3V**		6.5
-	**VIN_3.3**	-	**VIN_3.3**	15	Jx1	16	**3.3V**		7.5
AA13	B13_L3_P		MIO45	17	Jx1	18	SD_D3	-	8.5
AB13	B13_L3_N		MIO44	19	Jx1	20	SD_D2	-	9.5
Y12	B13_L11_N		MIO43	21	Jx1	22	SD_D1	-	10.5
Y11	B13_L11_P		MIO42	23	Jx1	24	SD_D0	-	11.5
AA11	B13_L9_N		MIO41	25	Jx1	26	SD_CMD	-	12.5
AA10	B13_L9_P		MIO40	27	Jx1	28	SD_CLK	-	13.5
-	**GND**	**-**	**GND**	29	Jx1	30	**GND**		14.5
E22	B16_L22_P	W12	B13_L3_P	31	Jx1	32	FMC_SCL	FMC C30	15.5
E21	B16_L22_N	W13	B13_L3_N	33	Jx1	34	FMC_SDA	FMC C31	16.5
G22	B16_L24_N	U11	B13_L5_P	35	Jx1	36	FMC_LA12_P	FMC G15	17.5
G21	B16_L24_P	U12	B13_L5_N	37	Jx1	38	FMC_LA12_N	FMC G16	18.5
-	**1.8V_OUT**	-	**1.8V_OUT**	39	Jx1	40	**1.8V**		19.5
E21	B16_L23_P	V15	B13_L2_P	41	Jx1	42	SD_SW	-	20.5
D21	B16_L23_N	W15	B13_L2_N	43	Jx1	44	*not connected*		21.5
F18	B16_L15_P	R17	B13_L19_P	45	Jx1	46	FMC_LA03_P	FMC G9	22.5
E18	B16_L15_N	T17	B13_L19_N	47	Jx1	48	FMC_LA03_N	FMC G10	23.5
C22	B16_L20_P	V13	B13_L1_P	49	Jx1	50	FMC_LA04_P	FMC H10	24.5
B22	B16_L20_N	V14	B13_L1_N	51	Jx1	52	FMC_LA04_N	FMC H11	25.5
-	**GND**	**-**	**GND**	53	Jx1	54	**GND**		26.5
B21	B16_L21_P	AB13	B13_L9_P	55	Jx1	56	FMC_LA08_P	FMC G12	27.5
A21	B16_L21_N	AB14	B13_L9_N	57	Jx1	58	FMC_LA08_N	FMC G13	28.5
C18	B16_L13_P	Y15	B13_L12_N	59	Jx1	60	FMC_CLK0_P	FMC H4	29.5

C19	B16_L13_N	Y14	B13_L12_P	61	Jx1	62	FMC_CLK0_N	FMC H5	30.5
-	**GND**	-	**GND**	63	Jx1	64			31.5
E19	B16_L14_P	AA15	B13_L11_N	65	Jx1	66	FMC_LA01_P	FMC D8	32.5
D19	B16_L14_N	AA14	B13_L11_P	67	Jx1	68	FMC_LA01_N	FMC D9	33.5
C15	B16_L3_N	AB16	B13_L17_P	69	Jx1	70	FMC_LA13_P	FMC D17	34.5
C14	B16_L3_P	AB17	B13_L17_N	71	Jx1	72	FMC_LA13_N	FMC D18	35.5
-	**GND**	-	**GND**	73	Jx1	74	**GND**		36.5
D17	B16_L12_P	Y19	B13_L13_N	75	Jx1	76	FMC_LA00_P	FMC G6	37.5
C17	B16_L12_N	Y18	B13_L13_P	77	Jx1	78	FMC_LA00_N	FMC G7	38.5
-	*not connected*	-	**VBAT_IN**	79	Jx1	80	VBAT	-	39.5
B13	B16_L8_N	AB18	B13_L16_P	81	Jx1	82	PHY_LED1	SEIC 48	40.5
C13	B16_L8_P	AB19	B13_L16_N	83	Jx1	84	PHY_LED2	SEIC 47	41.5
U18	B14_L18_N		MIO15	85	Jx1	86	UART_TX	SEIC 7	42.5
U17	B14_L18_P		MIO0	87	Jx1	88	RTC_INT#		43.5
-	JTAGSEL	-	JTAGSEL	89	Jx1	90	JTAGEN		44.5
Y21	B14_L9_P		MIO9	91	Jx1	92	HOST#	-	45.5
Y22	B14_L9_N		MIO11	93	Jx1	94	I2C0_SDA	-	46.5
T21	B14_L4_P		MIO10	95	Jx1	96	I2C0_SCL	-	47.5
U21	B14_L4_N		MIO13	97	Jx1	98	I2C1_SDA	-	48.5
R17	B14_L24_N		MIO12	99	Jx1	100	I2C1_SCL	-	49.5
									50
-	**GND**	-	**GND**	2	Jx1	1	**GND**		101
-	ETH_TD_P	-	PHY_MDI0_P	4	Jx1	3	PHY_MDI0_P	SEIC 54	102
-	ETH_TD_N	-	PHY_MDI0_N	6	Jx1	5	PHY_MDI0_N	SEIC 56	103
-	**GND**	-	**GND**	8	Jx1	7	**GND**		104
-	ETH_RD_P	-	PHY_MDI1_P	10	Jx1	9	PHY_MDI1_P	SEIC 58	105
-	ETH_RD_N	-	PHY_MDI1_N	12	Jx1	11	PHY_MDI1_N	SEIC 60	106
-	**3.3V_OUT**	-	*not connected*	14	Jx1	13	*not connected*		107
Y14	B13_L6_N	-	PHY_MDI2_P	16	Jx1	15	PHY_MDI2_P	SEIC 59	108
W14	B13_L6_P	-	PHY_MDI2_N	18	Jx1	17	PHY_MDI2_N	SEIC 57	109
-	**GND**	-	**GND**	20	Jx1	19	**GND**		110
AA14	B13_L5_N	-	PHY_MDI3_P	22	Jx1	21	PHY_MDI3_P	SEIC 55	111
Y13	B13_L5_P	-	PHY_MDI3_N	24	Jx1	23	PHY_MDI3_N	SEIC 53	112
-	**GND**	-	**GND**	26	Jx1	25	**GND**		113
-	EN1	-	EN1	28	Jx1	27			114
-	PGOOD	-	PGOOD	30	Jx1	29			115
-	MODE	-	MODE	32	Jx1	31	MODE	JP11	116
-	**GND**	-	**GND**	34	Jx1	33	**GND**		117
B20	B16_L16_P	U13	B13_L6_P	36	Jx1	35	FMC_LA02_P	FMC H7	118

A20	B16_L16_N	U14	B13_L6_N	38	Jx1	37	FMC_LA02_N	FMC H8	119
C20	B16_L19_N	V11	B13_L4_P	40	Jx1	39	FMC_LA11_P	FMC H16	120
D20	B16_L19_P	W11	B13_L4_N	42	Jx1	41	FMC_LA11_N	FMC H17	121
-	**GND**	-	**GND**	44	Jx1	43	**GND**		122
A19	B16_L17_N	AA11	B13_L7_P	46	Jx1	45	FMC_LA06_P	FMC C10	123
A18	B16_L17_P	AB11	B13_L7_N	48	Jx1	47	FMC_LA06_N	FMC C11	124
F20	B16_L18_N	AA12	B13_L8_P	50	Jx1	49	FMC_LA05_P	FMC D11	125
F19	B16_L18_P	AB12	B13_L8_N	52	Jx1	51	FMC_LA05_N	FMC D12	126
-	**GND**	-	**GND**	54	Jx1	53	**GND**		127
A16	B16_L9_N	Y12	B13_L10_P	56	Jx1	55	FMC_LA07_P	FMC H13	128
A15	B16_L9_P	Y13	B13_L10_N	58	Jx1	57	FMC_LA07_N	FMC H14	129
B16	B16_L7_N	V16	B13_L23_P	60	Jx1	59	FMC_LA10_P	FMC C14	130
B15	B16_L7_P	W16	B13_L23_N	62	Jx1	61	FMC_LA10_N	FMC C15	131
-	**GND**	-	**GND**	64	Jx1	63	**GND**		132
B17	B16_L11_P	AA17	B13_L14_N	66	Jx1	65	FMC_CLK1_P	FMC G3	133
B18	B16_L11_N	AA16	B13_L14_P	68	Jx1	67	FMC_CLK1_N	FMC G4	134
A14	B16_L10_N	Y17	B13_L24_N	70	Jx1	69	FMC_LA14_P	FMC C18	135
A13	B16_L10_P	W17	B13_L24_P	72	Jx1	71	FMC_LA14_N	FMC C19	136
-	**GND**	-	**GND**	74	Jx1	73	**GND**		137
D16	B16_L5_N	AA19	B13_L18_P	76	Jx1	75	FMC_LA15_P	FMC H19	138
E16	B16_L5_P	AA20	B13_L18_N	78	Jx1	77	FMC_LA15_N	FMC H20	139
E17	B16_L2_N	W18	B13_L21_N	80	Jx1	79	*not connected*		140
F16	B16_L2_P	V18	B13_L21_P	82	Jx1	81	*not connected*		141
-	**GND**	-	**GND**	84	Jx1	83	**GND**		142
D15	B16_L6_N	V19	B13_L20_N	86	Jx1	85	*not connected*		143
D14	B16_L6_P	U19	B13_L20_P	88	Jx1	87	LED1	SEIC 46	144
-	**GND**	-	**GND**	90	Jx1	89	**GND**		145
P16	B14_L24_P		MIO14	92	Jx1	91	UART_RX	SEIC 8	146
E14	B16_L4_N	AB21	B13_L15_P	94	Jx1	93	*not connected*		147
E13	B16_L4_P	AB22	B13_L15_N	96	Jx1	95	*not connected*		148
F14	B16_L1_N	U17	B13_L22_P	98	Jx1	97	*not connected*		149
F13	B16_L1_P	U18	B13_L22_N	##	Jx1	99	LED2	SEIC 44	150
									199
-	**VCCIO_B13_IN**	-	*not connected*	1	Jx2	2	**VCCIO34**	JP7	200.5
-	**VCCIO_B13_IN**	-	*not connected*	3	Jx2	4	**VCCIO34**	JP7	201.5
-	*not connected*	-	**VCCIO_B34_IN**	5	Jx2	6	**VCCIO34**	JP7	202.5
-	**VCCIO_B15_IN**	-	**VCCIO_B35_IN**	7	Jx2	8	**VCCIO35**	JP8	203.5
-	**VCCIO_B15_IN**	-	**VCCIO_B35_IN**	9	Jx2	10	**VCCIO35**	JP8	204.5
AA21	B14_L8_N	R3	B34_L17_P	11	Jx2	12	TTL3	JP3 8	205.5

AA20	B14_L8_P	R2	B34_L17_N	13	Jx2	14	TTL2	JP3 6	206.5
AB18	B14_L17_N	P3	B34_L18_P	15	Jx2	16	TTL1	JP3 7	207.5
AA18	B14_L17_P	P2	B34_L18_N	17	Jx2	18	TTL0	JP3 5	208.5
-	**1.5V_OUT**	-	**1.5V_OUT**	19	Jx2	20	*not connected*		209.5
V18	B14_L14_P	K4	B34_L11_P	21	Jx2	22	TTLN	JP3 1	210.5
V19	B14_L14_N	K3	B34_L11_N	23	Jx2	24	TTLP	JP3 2	211.5
Y18	B14_L13_P	L5	B34_L12_P	25	Jx2	26	HDMI_INT	SEIC 83	212.5
Y19	B14_L13_N	L4	B34_L12_N	27	Jx2	28	CT_HPD	SEIC 73	213.5
-	*not connected*	-	*not connected*	29	Jx2	30	**GND**		214.5
V17	B14_L16_P	J2	B34_L8_P	31	Jx2	32	LS_OE	SEIC 74	215.5
W17	B14_L16_N	J1	B34_L8_N	33	Jx2	34	CEC_CLK	SEIC 75	216.5
AA19	B14_L15_P	J5	B34_L7_P	35	Jx2	36	WIRE1	-	217.5
AB20	B14_L15_N	K5	B34_L7_N	37	Jx2	38	PPS1	J5	218.5
-	**GND**	-	**GND**	39	Jx2	40	**GND**		219.5
L16	B15_L23_P	E3	B35_L21_N	41	Jx2	42	FMC_LA09_P	FMC D14	220.5
K16	B15_L23_N	E4	B35_L21_P	43	Jx2	44	FMC_LA09_N	FMC D15	221.5
K13	B15_L19_P	B6	B35_L8_N	45	Jx2	46	FMC_LA20_N	FMC G22	222.5
K14	B15_L19_N	B7	B35_L8_P	47	Jx2	48	FMC_LA20_P	FMC G21	223.5
-	**GND**	-	**GND**	49	Jx2	50	**GND**		224.5
J20	B15_L11_P	C6	B35_L11_P	51	Jx2	52	FMC_LA18_P	FMC C22	225.5
J21	B15_L11_N	C5	B35_L11_N	53	Jx2	54	FMC_LA18_N	FMC C23	226.5
J14	B15_L3_P	E7	B35_L1_N	55	Jx2	56	AD0N	SEIC 36	227.5
H14	B15_L3_N	F7	B35_L1_P	57	Jx2	58	AD0P	SEIC 34	228.5
-	**GND**	-	**GND**	59	Jx2	60	**GND**		229.5
N19	B15_L17_N	D8	B35_L3_N	61	Jx2	62	AD1N	SEIC 35	230.5
N18	B15_L17_P	E8	B35_L3_P	63	Jx2	64	AD1P	SEIC 33	231.5
M18	B15_L16_P	C8	B35_L7_P	65	Jx2	66	FMC_LA26_P	FMC D26	232.5
L18	B15_L16_N	B8	B35_L7_N	67	Jx2	68	FMC_LA26_N	FMC D27	233.5
-	**GND**	-	**GND**	69	Jx2	70	**GND**		234.5
H13	B15_L1_P	G7	B35_L4_N	71	Jx2	72	FMC_LA16_N	FMC G19	235.5
G13	B15_L1_N	G8	B35_L4_P	73	Jx2	74	FMC_LA16_P	FMC G18	236.5
G16	B15_L2_N	H3	B35_L19_N	75	Jx2	76	FMC_LA27_P	FMC C26	237.5
G15	B15_L2_P	H4	B35_L19_P	77	Jx2	78	FMC_LA27_N	FMC C27	238.5
-	**GND**	-	**GND**	79	Jx2	80			239.5
G17	B15_L4_P	E5	B35_L5_N	81	Jx2	82	FMC_LA24_P	FMC H28	240.5
G18	B15_L4_N	F5	B35_L5_P	83	Jx2	84	FMC_LA24_N	FMC H29	241.5
H15	B15_L5_N	F6	B35_L6_N	85	Jx2	86	FMC_LA28_P	FMC H31	242.5

J15	B15_L5_P	G6	B35_L6_P	87	Jx2	88	FMC_LA28_N	FMC H32	243.5
J16	B15_IO0	H6	B35_IO0	89	Jx2	90	FMC_LA32_N	FMC H38	244.5
-	**JTAG_VREF**	-	**JTAG_VREF**	91	Jx2	92	VCCJTAG		245.5
	TMS		TMS	93	Jx2	94	TMS		246.5
	TDI		TDI	95	Jx2	96	TDI		247.5
	TDO		TDO	97	Jx2	98	TDO		248.5
	TCK		TCK	99	Jx2	100	TCK		249.5
									250
-	**VIN_DCDC**	-	**VIN_DCDC**	2	Jx2	1	**5.0V**		301
-	**VIN_DCDC**	-	**VIN_DCDC**	4	Jx2	3	**5.0V**		302
-	**VIN_DCDC**	-	**VIN_DCDC**	6	Jx2	5	**5.0V**		303
-	**VIN_DCDC**	-	**VIN_DCDC**	8	Jx2	7	**5.0V**		304
-	**3.3V_OUT**	-	**3.3V_OUT**	10	Jx2	9	**3.3V_OUT**		305
-	**3.3V_OUT**	-	**3.3V_OUT**	12	Jx2	11	**3.3V_OUT**		306
AB22	B14_L10_N	M1	B34_L15_N	14	Jx2	13	TSPDIFIN	SEIC 65	307
AB21	B14_L10_P	M2	B34_L15_P	16	Jx2	15	TSPDIFOUT	SEIC 67	308
-	nRST	-	nRST	18	Jx2	17	TrenzRst#	-	309
-	**GND**	-	**GND**	20	Jx2	19	**GND**		310
W19	B14_L12_P	J7	B34_L2_P	22	Jx2	21	RS232_TX1	RS1 2	311
W20	B14_L12_N	J6	B34_L2_N	24	Jx2	23	RS232_TX2	RS1 5	312
U20	B14_L11_P	M7	B34_L6_N	26	Jx2	25	RS232_TX3	RS1 8	313
V20	B14_L11_N	M8	B34_L6_P	28	Jx2	27	RS232_RX1	RS1 3	314
-	**GND**	-	**GND**	30	Jx2	29	**GND**		315
K22	B15_L9_N	D1	B35_L16_P	32	Jx2	31	RS232_RX2	RS1 6	316
K21	B15_L9_P	C1	B35_L16_N	34	Jx2	33	RS232_RX3	RS1 9	317
G20	B15_L8_N	B1	B35_L18_N	36	Jx2	35	PCIeRST 18#	[JAB1 2]	318
H20	B15_L8_P	B2	B35_L18_P	38	Jx2	37			319
-	**GND**	-	**GND**	40	Jx2	39	**GND**		320
H22	B15_L7_N	A1	B35_L15_N	42	Jx2	41	CLK4	-	321
J22	B15_L7_P	A2	B35_L15_P	44	Jx2	43	CLK3	-	322
K18	B15_L13_P	B4	B35_L13_P	46	Jx2	45	CLK2	-	323
K19	B15_L13_N	B3	B35_L13_N	48	Jx2	47	CLK1	-	324
-	**GND**	-	**GND**	50	Jx2	49	**GND**		325
L19	B15_L14_P	D3	B35_L14_P	52	Jx2	51	FMC_LA19_P	FMC H22	326
L20	B15_L14_N	C3	B35_L14_N	54	Jx2	53	FMC_LA19_N	FMC H23	327
J19	B15_L12_P	D5	B35_L12_P	56	Jx2	55	FMC_LA17_P	FMC D20	328
H19	B15_L12_N	C4	B35_L12_N	58	Jx2	57	FMC_LA17_N	FMC D21	329
-	**GND**	-	**GND**	60	Jx2	59	**GND**		330
L21	B15_L10_N	F1	B35_L23_N	62	Jx2	61	FMC_LA22_P	FMC G24	331

M21	B15_L10_P	F2	B35_L23_P	64	Jx2	63	FMC_LA22_N	FMC G25	332
N20	B15_L18_P	D6	B35_L2_N	66	Jx2	65	FMC_LA21_P	FMC H25	333
M20	B15_L18_N	D7	B35_L2_P	68	Jx2	67	FMC_LA21_N	FMC H26	334
-	**GND**	-	**GND**	70	Jx2	69	**GND**		335
M13	B15_L20_P	E2	B35_L17_P	72	Jx2	71	FMC_LA23_P	FMC D23	336
L13	B15_L20_N	D2	B35_L17_N	74	Jx2	73	FMC_LA23_N	FMC D24	337
N22	B15_L15_P	H1	B35_L24_P	76	Jx2	75	FMC_LA25_P	FMC G27	338
M22	B15_L15_N	G1	B35_L24_N	78	Jx2	77	FMC_LA25_N	FMC G28	339
-	**GND**	-	**GND**	80	Jx2	79	**GND**		340
H18	B15_L6_N	A6	B35_L9_N	82	Jx2	81	FMC_LA29_P	FMC G30	341
H17	B15_L6_P	A7	B35_L9_P	84	Jx2	83	FMC_LA29_N	FMC G31	342
K17	B15_L21_P	G2	B35_L22_N	86	Jx2	85	FMC_LA31_P	FMC G33	343
J17	B15_L21_N	G3	B35_L22_P	88	Jx2	87	FMC_LA31_N	FMC G34	344
-	**GND**	-	**GND**	90	Jx2	89	**GND**		345
M16	B15_L24_N	A4	B35_L10_N	92	Jx2	91	FMC_LA30_P	FMC H34	346
M15	B15_L24_P	A5	B35_L10_P	94	Jx2	93	FMC_LA30_N	FMC H35	347
L15	B15_L22_N	F4	B35_L20_N	96	Jx2	95	FMC_LA33_P	FMC G36	348
L14	B15_L22_P	G4	B35_L20_P	98	Jx2	97	FMC_LA33_N	FMC G37	349
M17	B15_IO25	H5	B35_IO25	##	Jx2	99	FMC_LA32_P	FMC H37	350
									399
T16	B13_L17_P	-	SGMII_TX_N	1	Jx3	2	SOUT_N	SEIC 2	400.5
U16	B13_L17_N	-	SGMII_TX_P	3	Jx3	4	SOUT_P	SEIC 4	401.5
-	**GND**	-	**GND**	5	Jx3	6	**GND**		402.5
A4	MGT_TX0_N	AB3	MGT_TX0_N	7	Jx3	8	PE1RXN0	-	403.5
B4	MGT_TX0_P	AA3	MGT_TX0_P	9	Jx3	10	PE1RXP0	-	404.5
-	**GND**	-	**GND**	11	Jx3	12	**GND**		405.5
C5	MGT_TX1_N	Y4	MGT_TX1_N	13	Jx3	14	PE1RXN3	-	406.5
D5	MGT_TX1_P	W4	MGT_TX1_P	15	Jx3	16	PE1RXP3	-	407.5
-	**GND**	-	**GND**	17	Jx3	18	**GND**		408.5
A6	MGT_TX2_N	AB5	MGT_TX2_N	19	Jx3	20	SATA_TRZ_TX_N	[SEIC 21]	409.5
B6	MGT_TX2_P	AA5	MGT_TX2_P	21	Jx3	22	SATA_TRZ_TX_P	[SEIC 23]	410.5
-	**GND**	-	**GND**	23	Jx3	24			411.5
C7	MGT_TX3_N	Y2	MGT_TX3_N	25	Jx3	26	FMC_TRZ_TX_N	FMC C3	412.5
D7	MGT_TX3_P	W2	MGT_TX3_P	27	Jx3	28	FMC_TRZ_TX_P	FMC C2	413.5

-	**GND**	-	**GND**	29	Jx3	30	**GND**		414.5
E10	MGT_CLK1_N	V9	MGT_CLK0_N	31	Jx3	32	PCLKP0		415.5
F10	MGT_CLK1_P	U9	MGT_CLK0_P	33	Jx3	34	PCLKN0		416.5
-	**GND**	-	**GND**	35	Jx3	36	**GND**		417.5
V10	B13_L10_P	P6	B34_L20_P	37	Jx3	38	HDMI_D11	SEIC 87	418.5
W10	B13_L10_N	P5	B34_L20_N	39	Jx3	40	HDMI_D9	SEIC 91	419.5
T14	B13_L15_P	N4	B34_L21_P	41	Jx3	42	HDMI_D7	SEIC 95	420.5
T15	B13_L15_N	N3	B34_L21_N	43	Jx3	44	HDMI_D5	SEIC 98	421.5
-	**GND**	-	**GND**	45	Jx3	46	**GND**		422.5
P19	B14_L5_P	-	OTG-D_P	47	Jx3	48	OTG_D_P	SEIC 13	423.5
R19	B14_L5_N	-	OTG-D_N	49	Jx3	50	OTG_D_N	SEIC 15	424.5
R18	B14_L20_P	-	OTG-ID	51	Jx3	52	OTG_ID	SEIC 16	425.5
T18	B14_L20_N	-	VBUS_V_EN	53	Jx3	54	VBUS_V_EN	SEIC 14	426.5
-	*not connected*	-	USB-VBUS	55	Jx3	56	USB_VBUS	SEIC 12	427.5
V13	B13_L13_P	T2	B34_L13_P	57	Jx3	58	HDMI_HSYNC	SEIC 80	428.5
V14	B13_L13_N	T1	B34_L13_N	59	Jx3	60	HDMI_VSYNC	SEIC 78	429.5
									499
U15	B13_L14_P	-	SGMII_RX_N	2	Jx3	1	SIN_N	SEIC 1	501
V15	B13_L14_N	-	SGMII_RX_P	4	Jx3	3	SIN_P	SEIC 3	502
-	**GND**	-	**GND**	6	Jx3	5	**GND**		503
A8	MGT_RX0_N	AB7	MGT_RX0_N	8	Jx3	7	PE1TXN0	-	504
B8	MGT_RX0_P	AA7	MGT_RX0_P	10	Jx3	9	PE1TXP0	-	505
-	**GND**	-	**GND**	12	Jx3	11	**GND**		506
C11	MGT_RX1_N	Y8	MGT_RX1_N	14	Jx3	13	PE1TXN3	-	507
D11	MGT_RX1_P	W8	MGT_RX1_P	16	Jx3	15	PE1TXP3	-	508
-	**GND**	-	**GND**	18	Jx3	17	**GND**		509
A10	MGT_RX2_N	AB9	MGT_RX2_N	20	Jx3	19	SATA_TRZ_RX_N	[SEIC 22]	510
B10	MGT_RX2_P	AA9	MGT_RX2_P	22	Jx3	21	SATA_TRZ_RX_P	[SEIC 24]	511
-	**GND**	-	**GND**	24	Jx3	23	**GND**		512
C9	MGT_RX3_N	Y6	MGT_RX3_N	26	Jx3	25	FMC_TRZ_RX_N	FMC C7	513
D9	MGT_RX3_P	W6	MGT_RX3_P	28	Jx3	27	FMC_TRZ_RX_P	FMC C6	514
-	**GND**	-	**GND**	30	Jx3	29	**GND**		515
-	CLKIN2_N	-	CLKIN2_P	32	Jx3	31	FMC_TRZ_CK_P	FMC D4	516
-	CLKIN2_P	-	CLKIN2_N	34	Jx3	33	FMC_TRZ_CK_N	FMC D5	517
-	**GND**	-	**GND**	36	Jx3	35	**GND**		518
W15	B13_L16_P	R5	B34_L23_P	38	Jx3	37	HDMI_D10	SEIC 89	519
W16	B13_L16_N	R4	B34_L23_N	40	Jx3	39	HDMI_D8	SEIC 93	520
Y16	B13_L1_P	N1	B34_L16_P	42	Jx3	41	HDMI_D6	SEIC 97	521
AA16	B13_L1_N	P1	B34_L16_N	44	Jx3	43	HDMI_D4	SEIC 96	522

-	**GND**	-	**GND**	46	Jx3	45	**GND**		523
AA15	B13_L4_P	L2	B34_L10_P	48	Jx3	47	HDMI_D3	SEIC 94	524
AB15	B13_L4_N	L1	B34_L10_N	50	Jx3	49	HDMI_D2	SEIC 92	525
AB17	B13_L2_N	M4	B34_L22_P	52	Jx3	51	HDMI_D1	SEIC 90	526
AB16	B13_L2_P	M3	B34_L22_N	54	Jx3	53	HDMI_D0	SEIC 88	527
-	*not connected*	-	*not connected*	56	Jx3	55			528
W11	B13_L12_P	U2	B34_L14_P	58	Jx3	57	HDMI_DE	SEIC 78	529
W12	B13_L12_N	U1	B34_L14_N	60	Jx3	59	HDMI_CLK	SEIC 82	530