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VPX Test Platform User Manual

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Revision History

Revision	Date	Changes
0A	March 2015	First Draft release

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About This Manual

This manual consists of information to simplify your installation, configuration and operation of the VPX Test Platform board. *About this Manual* describes the contents of each chapter and includes document conventions and technical support information

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Chapters Overview

About This Manual - This chapter provides an overview of the chapters, document conventions, and technical support information.

Chapter 1 ***Introduction -*** This chapter provides a brief introduction to the VPX Test Platform. It also provides a list of reference documents whose information supplements this user manual.

Chapter 2 ***Product Overview -*** This chapter provides detailed functional information for the VPX Test Platform.

Chapter 3 ***Specifications -*** This chapter provides the specifications for the functional areas of the VPX Test Platform.

Chapter 4 ***Installation and Setup -*** This chapter includes instructions for unpacking and installing the VPX Test Platform.

Chapter 5 ***Operating Guide -*** This chapter provides information on proper operation of the VPX Test Platform.

Acronym List - This chapter expands abbreviations used in this manual.

Document Conventions

The following icons are used in this manual to emphasize setup or system information:

Icon	Use
	Alerts you to the important details regarding the setup and maintenance of your system.
	Alerts you to potential damage to the board during system setup and installation.

Technical Support

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1 Introduction

This chapter provides a brief introduction to the VPX Test Platform. It also provides a list of reference documents whose information supplements this user manual.

1.1 The VPX Test Platform

The VPX Test Platform is a 3U OpenVPX rack with a 3-slot backplane, power supply and fan. The open frame design of the rack makes it ideally suited for software, firmware and hardware development of 3U VPX modules. Its main purpose is to provide a development platform for the Parsec OpenVPX hardware like the **VF360**.

The 3-slot backplane has one payload slot and two peripheral slots with Fat Pipe (FP) connections between the payload slot and each peripheral slot.

The VPX Test Platform is available in both air-cooled and conduction cooled versions.

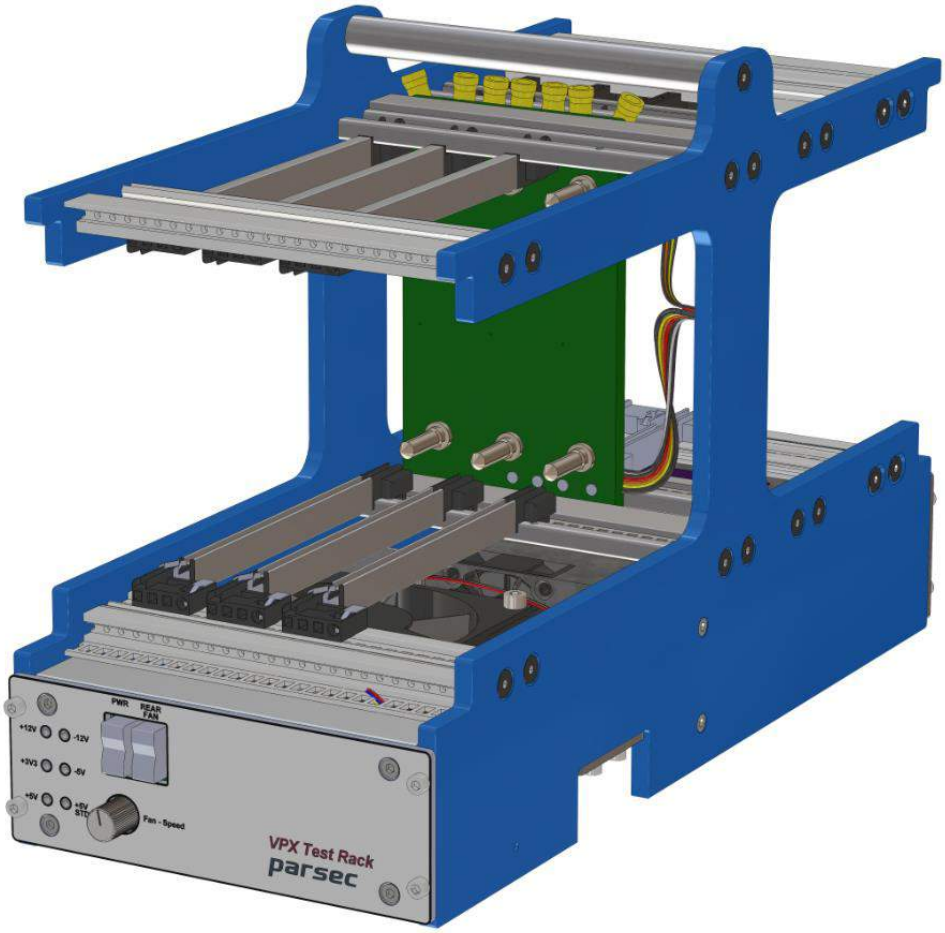

Figure 1: Air cooled VPX Test Platform

1.2 Features

- 180W power supply
- Fan with speed control
- 3-slot OpenVPX backplane (BKP3-CEN03-15.2.9-n)
- 3 front slots with wide guides
- 3 rear slots
- Open frame architecture for easy debugging and development
- COMPANION MODULES typically used with the VPX Test Platform

  VF360 3U FPGA and DSP OpenVPX Processing Module.

  VR300 RTM with USB-Blaster II, XDS100 and Ethernet (via SFP)

  FM500 FMC with USB-Blaster II, XDS100 and mini-SAS interfaces

  FM510 Video and IO FMC

1.3 Product Applications

The VPX Test Platform is targeted at the following applications:

- OpenVPX Hardware, Software and Firmware development
- VF360 application development
- Debugging of OpenVPX applications using up-to 3 OpenVPX modules

1.4 Reference Documents

The following sources provide important reference information that may provide useful in achieving optimal operation of the VPX Test Platform:

[1] VF360 User Manual

[2] FM500 FMC Product Brief

[3] FM510 FMC Product Brief

[4] VR300 RTM Product Brief

2 Product Overview

This chapter provides detailed functional information for the VPX Test Platform.

2.1 Overview of the VPX Test Platform

The VPX Test Platform is a 3U OpenVPX test platform used for application development of 3U OpenVPX modules, typically the Parsec VF360 module [1].

Figure 2 shows the VPX Test Platform front and rear views in its standard configuration.

- VF360 3U OpenVPX module in the system slot (left)
- VR300 Rear Transition Module (RTM) in the rear slot (left)

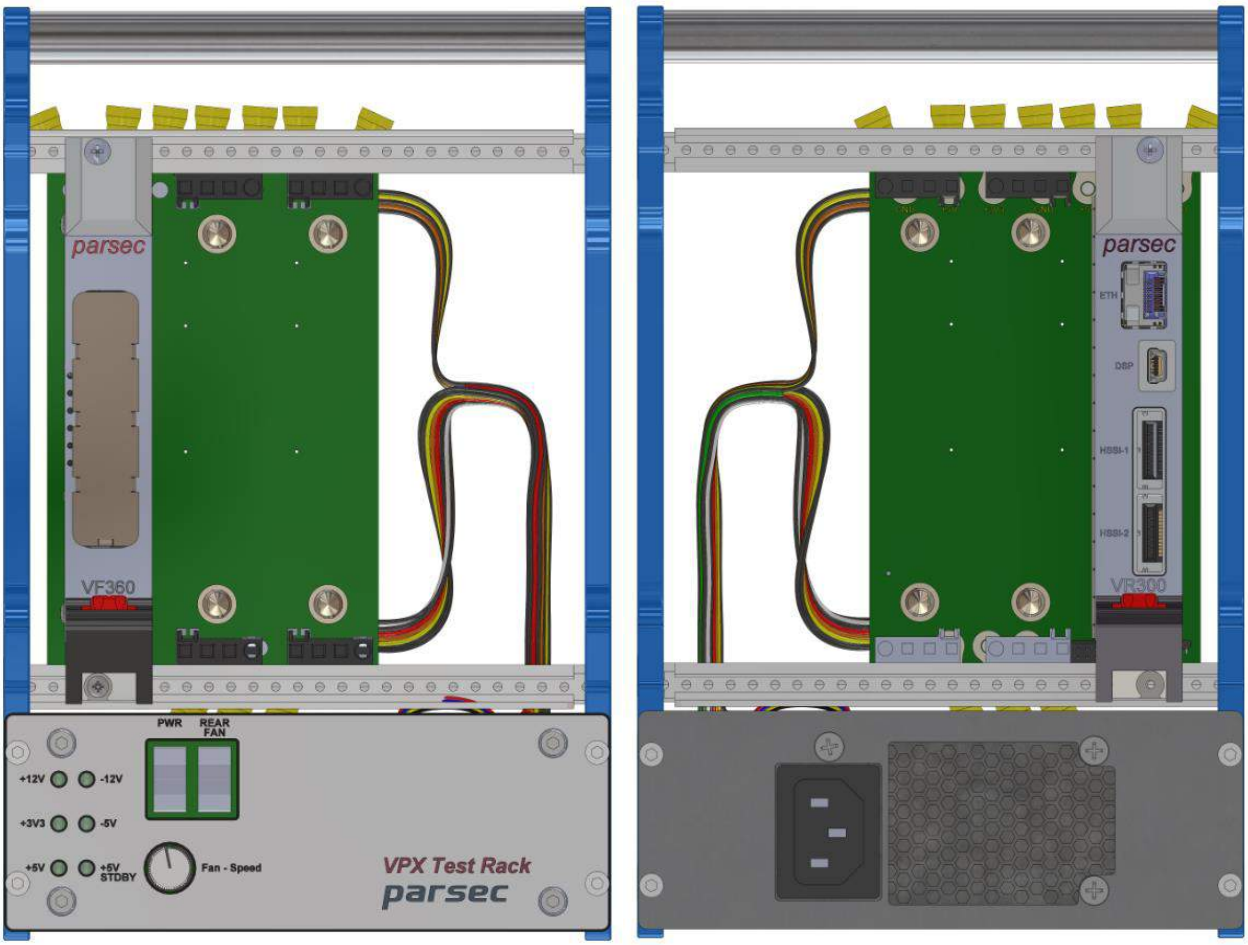

Figure 2: VPX Test Platform front and rear views

2.2 Control panel

The VPX Test Platform control panel is shown in Figure 3 and provides the following functions:

- Power switch to enable power to the backplane
- Rear Fan switch (no function), the main fan is always on
- Fan speed control knob to control the amount of air-flow to the VPX modules
- LEDs indicating active power rails

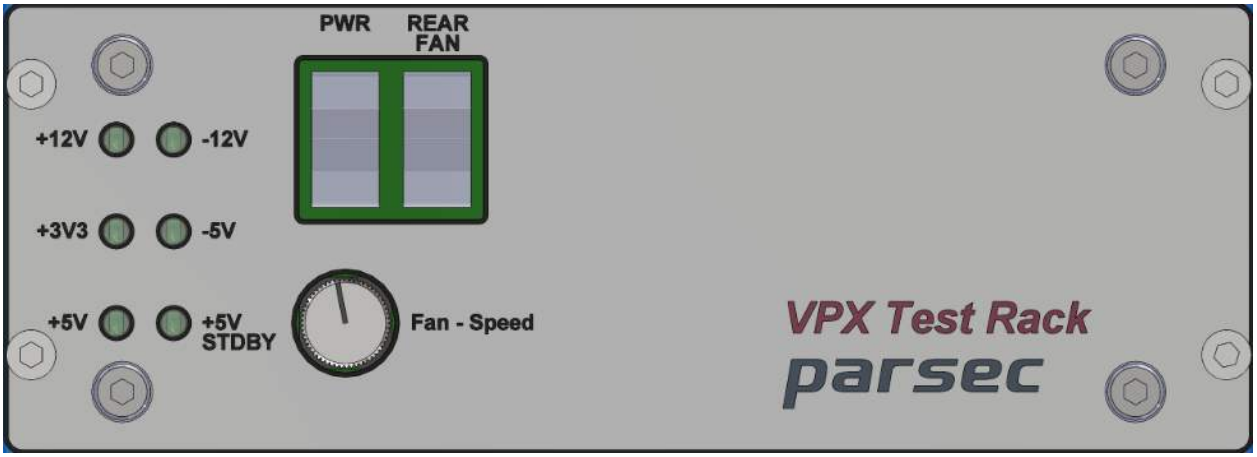

Figure 3: VPX Test Platform Control Panel

2.3 OpenVPX Backplane

The VPX Test Platform houses a 3-slot OpenVPX backplane (**BKP3-CEN03-15-2-9-4**) with one Payload slot and two Peripheral slots as shown in Figure 4.

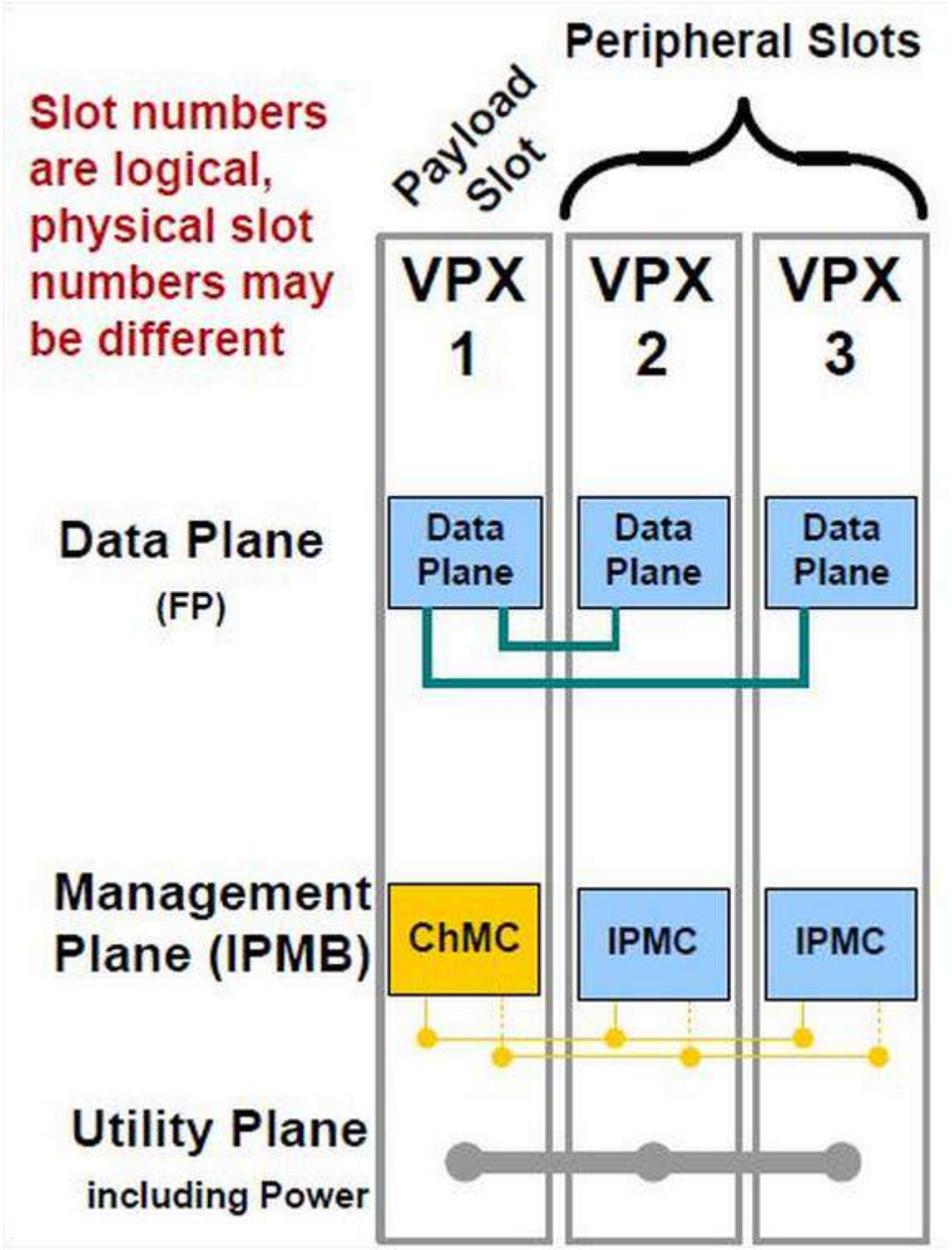

Figure 4: VPX Test Platform Backplane diagram

VPX1 DP01 is routed VPX2 DP01 and VPX1 DP02 is routed VPX3 DP01. All Control Plane connections are routed through to the rear slot.

The VPX Test Platform supports the following slot profiles:

- VPX1 Payload (and System) slot
  - SLT3-PAY-2F-14.2.17 (standard)
  - SLT3-PAY-3F2U.14.2.13 (VF360)
- VPX2 and VPX3 Peripheral slots
  - SLT3-PER-1F-14.3.2 (standard)
  - SLT3-PER-2F-14.3.1 and SLT3-PAY-2F-14.2.17 (optional)
  - SLT3-PAY-3F2U.14.2.13 (VF360)


Other slot profiles might also be supported BUT should first be confirmed with Parsec.

2.4 VR300 Rear Transition Module (RTM)

The VR300 Rear Transition Module is typically used with the VF360 in the VPX Test Platform. It is plugged into the rear IO slot and provides the following VF360 rear interfaces:

Refer to [4] for detail.

Figure 5: VR300 Rear Transition Module

- **ETH** => 1GBps Ethernet connection from the DSP via a SFP cage.
- **DSP** => XDS100v1 DSP debugger via mini USB connector
  - Connect to TI TMS320C667X DSP
  - In Circuit Emulation (ICE)
  - USB Serial Port for debugging
  - Compatible with Code Composer Studio
- **FPGA** => ALTERA USB-Blaster II via mini USB connector (on PCB next to VPX connector)
  - Connects to Stratix® V FPGA
  - SignalTap® II Logic Analyzer
  - FPGA configuration and EPCQ Programming
- **HSSI-1 and HSSI-2** => Two 4X HSSI connections to FPGA via two mini-SAS connectors
  - Connects to Stratix® V FPGA on X8d[1:4] and X12d[1:4]

2.5 FM500 Test FMC

The FM500 can be used with the VF360 in the VPX Test Platform. The **FM500** FMC is plugged onto the VF360 FMC site and provides the following front panel VF360 interfaces: Refer to [2] for detail.

Figure 6: FM500 Test FMC

- **DSP** => XDS100v1 DSP debugger via mini USB connector
  - Connect to TI TMS320C667X DSP
  - In Circuit Emulation (ICE)
  - USB Serial Port for debugging
  - Compatible with Code Composer Studio
- **FPGA** => ALTERA USB-Blaster II via mini USB connector
  - Connects to Stratix® V FPGA
  - SignalTap® II Logic Analyzer
  - FPGA configuration and EPCQ Programming
- **HSSI** => One 4X HSSI connection to FPGA via a mini-SAS connector
  - Connects to Stratix® V FPGA on FMC_DP[0:3]

2.6 FM510 Video and IO FMC

The FM510 can be used with the VF360 in the VPX Test Platform. The **FM510** FMC is plugged onto the VF360 FMC site and provides the following front panel VF360 interfaces: Refer to [3] for detail.

Figure 7: FM510 Video and IO FMC

- **Digital Video** => SDI video for FM510-DD
  - SDI video output on Vout
  - SDI video input on Vin
- **Analogue Video** => Analogue video for FM510-AA
  - Analogue video output on Vout
  - Analogue video input on Vin
- **IO** => High-density Samtec connector (LSHM-150-01-L-RH-A-S-K-TR)
  - 10x full duplex RS422 interfaces
  - 4x half-duplex RS485 interfaces
  - 4x half-duplex CAN interfaces
  - 4x isolated digital outputs (external 5-30V)
  - 4x isolated digital inputs (12-30V)
  - 2x Audio inputs (stereo)
  - 2x Audio outputs (stereo)

3 Specifications

This chapter provides the specifications for the functional areas of the VPX Test Platform.

3.1 General Specifications

The VPX Test Platform supports the following slot profiles:

- VPX1 Payload (and System) slot
  - SLT3-PAY-2F-14.2.17 (standard)
  - SLT3-PAY-3F2U.14.2.13 (VF360)
- VPX2 and VPX3 Peripheral slots
  - SLT3-PER-1F-14.3.2 (standard)
  - SLT3-PER-2F-14.3.1 and SLT3-PAY-2F-14.2.17 (optional)
  - SLT3-PAY-3F2U.14.2.13 (VF360)

Other slot profiles might also be supported BUT MUST first be confirmed with Parsec.

3.2 Environmental Specification

3.2.1 Temperature

Operating…….…… 0 to 50 degrees Celsius

The **fan** MUST always be switch on and running at ½ of the maximum speed.
For high power applications the fan must run at FULL speed.

3.2.2 Dimensions

Size (PCB) ……..…… 140 mm x 190 mm x 315 mm

Weight (AC)……. TBD g

3.3 Power Supply

The VPX Test Platform PSU supports maximum supply rail currents as shown in Table 1, with a total of 180W.

Table 1: VPX Test Platform Power supply maximum currents

PSU Rail	Minimum load	Maximum load
Vs1 (12V)	0.3 A	10 A
Vs2 (3.3V)	0.1 A	10 A
Vs3 (5V)	0.2 A	14 A
Maximum Power		180 W

3.4 Ordering Information

The VPX Test Platform ordering information is shown below

VF360 Test Platform – AC (Air cooled rack with 3-slot backplane)

VF360 Test Platform – CC (Conduction cooled rack with 3-slot backplane)

Contact factory for other order options

4 Installation and Setup

This chapter includes instructions for unpacking and installing the VPX Test Platform.

4.1 Unpacking the product

Before unpacking the product, note the following guidelines:

1. Check the shipping carton for damage. If the product's shipping carton is damaged upon arrival, request that the carrier's agent be present during unpacking and inspection of the board.
2. Once unpacked, the board should be inspected carefully for physical damage, loose components etc. In the event of the board arriving at the customer's premises in an obviously damaged condition, Parsec or its authorized agent should be notified immediately.
3. Make sure that the area designated for unpacking the product is a **static electricity controlled environment**. Unpack the VPX Test Platform *only* on a ground conductive pad using an anti-static wrist strap grounded to the pad.
4. If moving the VPX Test Platform is necessary, move it in an ESD protective container.
   Note: The VPX Test Platform is shipped in an ESD protective container.

4.2 Inserting/removing the VF360 or VR300 modules

Once the VPX Test Platform has been unpacked, ensure that VR300 (if ordered) is present in the rear right slot (as seen from the rear) and that the VF360 is present in the front left slot (VPX 1).

Before removing the VF360 or VR300, check the anti-static precautions listed in 4.1 above.

Remove the two screws at the top and the bottom of the module front panel. The bottom screw is located below the ejector handle.

Remove or insert the module by means of the ejector handle.

It is strongly advised that, when handling the VPX Test Platform and its associated components, the user should wear an earth strap to prevent damage to the board as a result of electrostatic discharge.

4.3 Powering the VPX Test Platform

Before switching on the VPX Test Platform power, do the following:

Check that the AC power cable is plugged in at the rear of the rack

Ensure that the VF360 and VR300 modules are completely inserted into their respective slots

Ensure that the fan speed knob at ½ of the maximum speed

Note that the fan cannot be switched off.

Switch on the rack at with the switch marked **PWR**

5 Operating Guide

This chapter provides information on proper operation of the VPX Test Platform.

5.1 Operation

After the VPX Test Platform is switched on, the fan should start blowing and the Test Rack control panel LEDs should be illuminated.

Refer to the **VF360** User Manual [1] for detail on its operation.

5.2 Status Indicators

The VPX Test Platform Control panel has six LEDs. The LED functions are shown in Table 2.

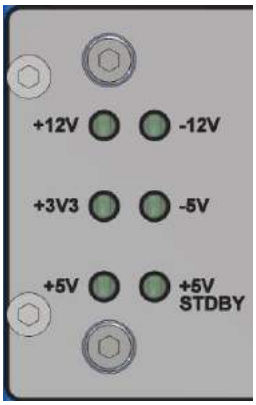

Table 2: Control panel LED indicators

Position	LED	Status	Status description
Left top	+12V	Green	12V rail OK
Left middle	+3V3	Green	3.3V rail OK
Left bottom	+5V	Green	5V rail OK
Right top	-12V	Green	-12V rail OK (not used)
Right middle	-5V	Off	Not present
Right bottom	+5V STDBY	Green	5V standby rail OK (not used)

5.3 FM510 installation

It is strongly advised that, when handling the VPX Test Platform, the VF360/FM500 and its associated components, the user should wear an earth strap to prevent damage to the board as a result of electrostatic discharge.

Ensure that the **FM510** is plugged onto the **VF360** and that the VF360 is inserted into the VPX Test Platform.

Ensure that the four FM510 stand-off screws that secure the FM510 onto the VF360 are inserted (through the bottom of the VF360) and fastened.

Ensure that the FM510 Loopback board is plugged into the FM510 IO connector, as shown in Figure 8.

Figure 8: FM510 Loopback board plugged into FM510

The connections on the Loopback board are shown in Figure 9. The ten RS422 links are looped back TX to RX. On the RS485 and CAN busses, links 0 and 2 are connected to links 1 and 3 respectively. The 4 discrete outputs are looped back to the 4 discrete inputs. The Loopback board has a regulator that generates 20V as supply voltage for the 4 Discrete IOs.

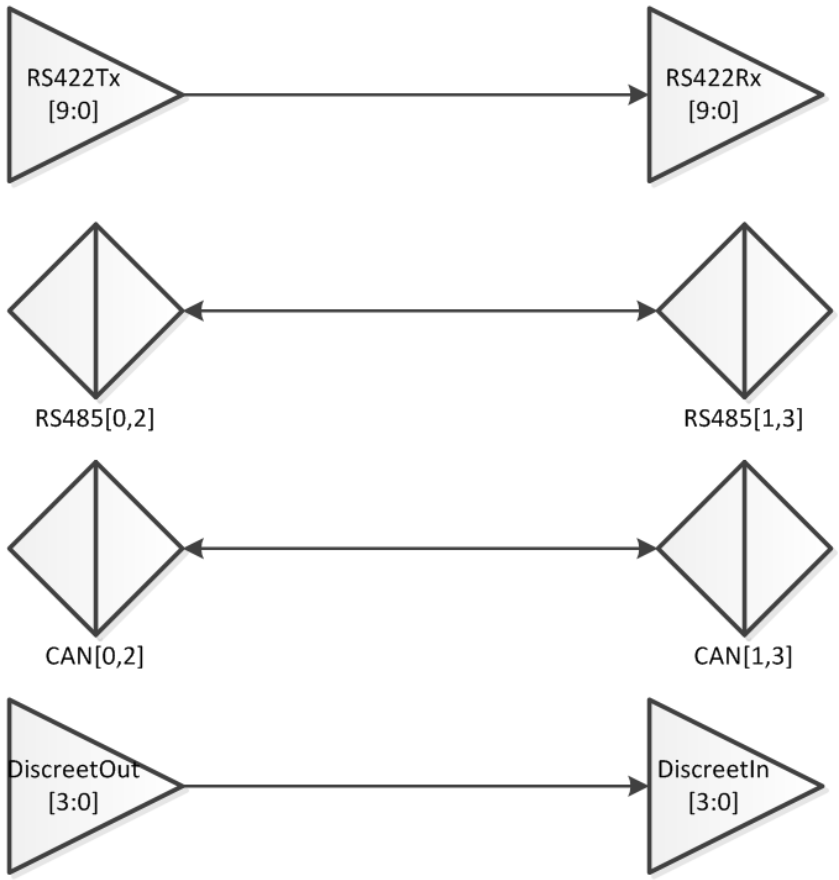

Figure 9: FM510 Loopback board connections

Refer to the VF3560 User Manual [1] for detail on using the VF360.

Plug a USB cable into the mini USB connector labelled **DSP** on the VR300, refer to § 2.4 for detail.

To connect to the DSP serial port, set-up PuTTY (or other terminal emulator) to 115200 baud, 8N1 with no flow control.

When powering the VPX Test Platform while connected to PuTTY, the Linux booting information should be displayed in the terminal window.

Switch on the VPX Test Platform power.

5.4 FM510 PCIe Test application

Type **lspci** at the terminal window prompt to list the devices detected on the PCIe bus. As a minimum the VF360 PLX PCIe Switch and the ALTERA FPGA should be displayed.

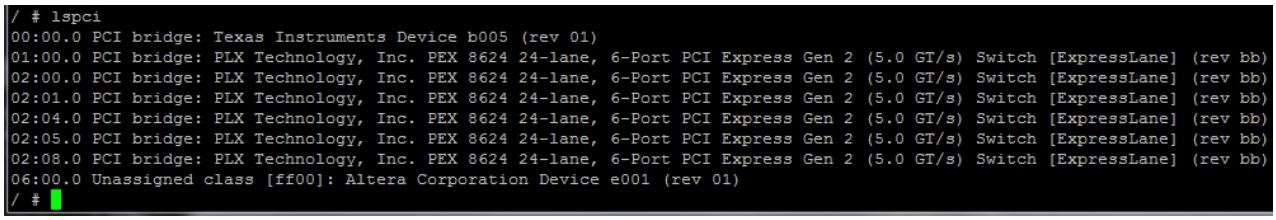

Figure 10: **lspci** terminal window

Change directory to the Test application:
"cd /root/pci04"

Load the PCIe driver:
"./load.sh"

Run the test application:
"./pci04_test /dev/parsec/pci04_e001_<SN>" where <SN> is the serial number of the VF360

e.g. "./pci04_test /dev/parsec/pci04_e001_E8376"

Press "**h**" at any time to display the menu commands

Press "**F**" twice to enter the FM510 Tests menu

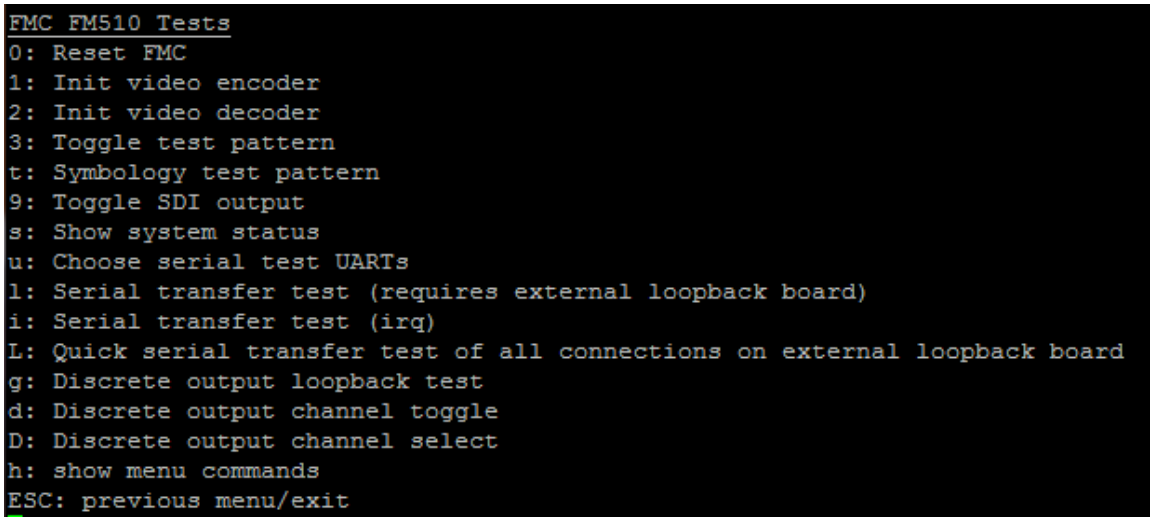

Figure 11: FM510 Tests menu

Press "**L**" to test the 18X UARTs on the Serial channels

The UARTs have the following logical to physical mapping on the IO connector

Serial [9:0] = RS422[9:0]

Serial [13:10] = RS485[3:0]

Serial [17:14] = CAN[3:0]

A specific Serial channel (UART) can be selected by pressing "**u**" multiple times.

The selected Serial channel can then be tested in detail (at all baud rates) by pressing "**l**"

Press “**g**” to test all 4 Discrete IOs.

A specific Discrete IO Serial can be selected by pressing “**D**” multiple times.

The selected Discrete IO can then be tested by pressing “**d**”. Observe the corresponding LED toggling on the Loopback board as d is pressed.

To test the SDI driver and receiver, connect the SDI loopback cable between Vin and Vout.

Press “s” to view the FM510 status.

```
FM510 status:
Reset           0
DVOscSel        0
SDI Output      0
Discrete OUT    1110
Discrete IN     0001
TxEn RS422      1111111111
TxEn RS485      1010
SDI Fault       1
SDI CD          0
```

If the SDI output is off (0), the SDI Fault will be high (1) and the SDI Carried Detect (SDI CD) on the receiver will be low (0).

Press “**9**” to enable (toggle) the SDI output and then press “**s**” again. Due to the SDI loopback connection, the SDI Fault will now be low (0) and the SDI Carried Detect (SDI CD) on the receiver will be high (1).

5.5 SYS/BIOS Test application

The test application can also run on SYS/BIOS, where the communication between the DSP and the FPGA is through the SRIO links (and not through PCIe)

The SYS/BIOS test applications takes ownership of the serial console and Linux loses access to the serial console once the application is run.

Change directory “**cd /root/sysbios**”

Run the SYS/BIOS application => “**mcoreloader 1 srio_demo_app.out**”

```
VF360 Test Application
v: Version of HW and FW
R: Test RAM IO
F: FMC Tests
h: show menu commands
ESC: previous menu/exit
```

Figure 12: SYS/BIOS Tests menu

Press “**F**” twice to enter the FM510 Tests menu and runs the same tests as with PCie Test application.

6 Acronym List

AC	Air cooled
CC	Conduction Cooled
DSP	Digital Signal Processor
ESD	Electrostatic Discharge
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
HSSI	High-Speed Serial Interface
JTAG	Joint Test Action Group
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCIe	PCI Express
PSU	Power supply
RTM	Rear Transition Module
SFP	Small form-factor pluggable

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