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SMT-FMC211

Quad DAC FMC

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Revision History

Issue	Changes Made	Date	Initials
1.0	First draft.	11/5/15 18/6/15	GKP
1.1	General update.	13/7/15	GKP
1.2	Changed to SMT-FMC211 from SMT-FMC3484	09/02/16	CH

Table of Contents

1 Introduction

This document describes the hardware features and some operational details of the SMT-FMC211.

Some discussion is made of how these features can be implemented with specific devices and how SMT-FMC211 can be expanded with a VITA57.1 FMC® compatible Daughter Cards for I/O expansion from the FPGA fabric.

1.1 Main Features

1.1.1 Hardware

This board consists of the following major hardware features:

1) Based on the Texas Instruments DAC3484 quad DAC
2) Artix-7 FPGA
3) 32-bit FPGA DDR3 Memory
4) LPC FMC
5) External/Internal clocks, triggers and sync for full flexibility

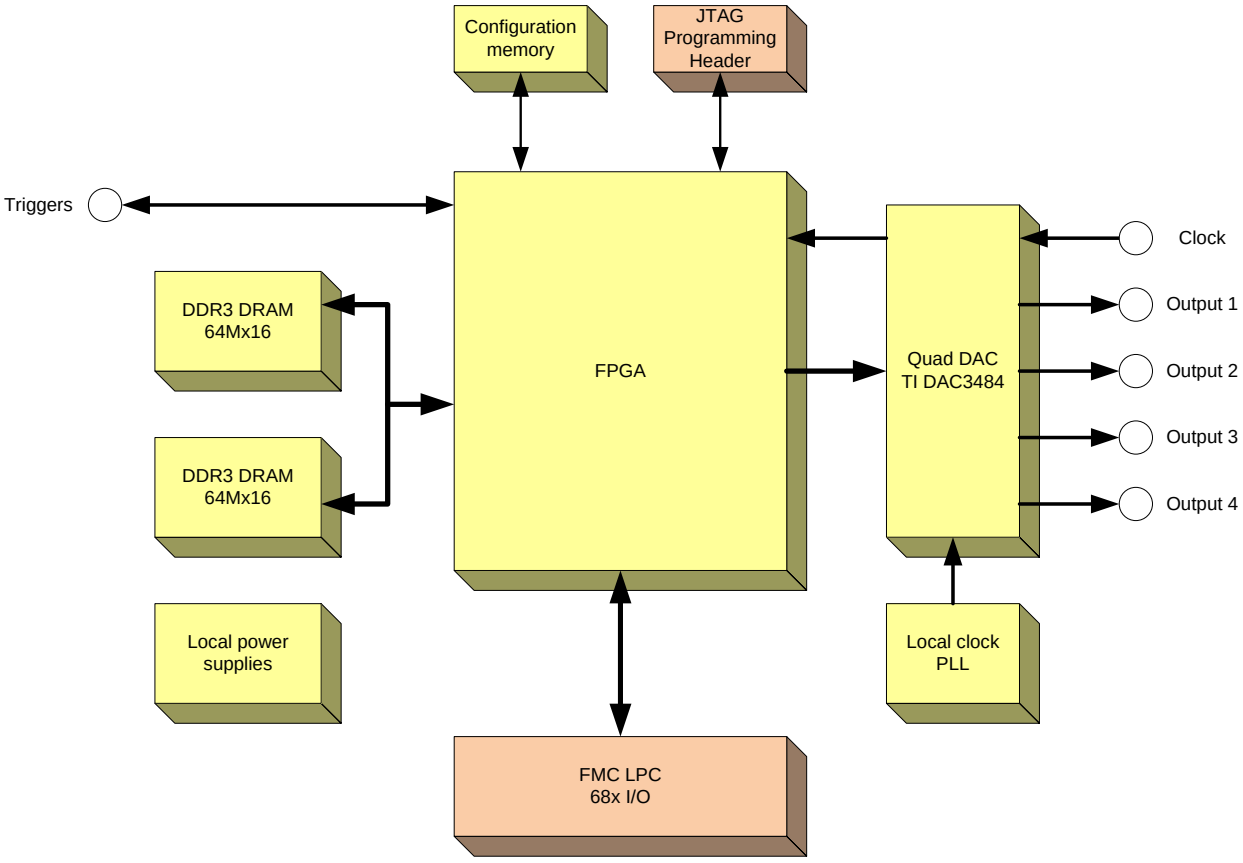
2 Notes

Several part numbers are described in the text, as HyperLinks. These are possible part numbers, and alternative devices may be designed in at a later date.

2.1 Abbreviations / Definitions

ADC	Analog to Digital Converter.
DDR & DDR3	Dual Data Rate. An interface mechanism where data is transferred on both rising and falling clock edges. DDR3 memory is lower power and higher performance than its predecessor, DDR2.
DRAM	Dynamic RAM.
DVI	Digital Visual Interface. When used on its own in this document it refers to the digital portion of the connector's signals.
DVI-D	Digital video data only.
DVI-I	Digital and analog (VGA) data.
EEPROM	Also called E^2PROM (or just E^2). Electrically erasable and programmable ROM.
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array.
GMII	Gigabit Media Independent Interface.
GPIO	General Purpose Input Output.
I^2C	Inter-integrated Circuit. A two wire low speed serial interface.
MAC	Media Access Control.
Magnetics	Commonly used to refer to the inductors and transformers within the Ethernet signalling to the RJ45 connector.
MCB	Memory Control Block. A Spartan 6 internal hard core.
MicroSD	Small from factor variant of SD.
PHY	Commonly used to refer to the device that interfaces to the physical layer.
PPS	Pulse Per Second. A high accuracy external clock input.
RAM	Random Access Memory.
RGMII	Reduced pin count GMII.
RJ45	Commonly used to refer to the 8-pin connector used in Ethernet communication.
SATA	Serial Advanced Technology Attachment. Refers to the high-speed serial signalling on hard disk drives.
SD	Secure Digital. Related to the format of some non-volatile memory cards.
SEIC	Sundance External Interface Connector.
SLB	Sundance Local Bus. Multiple 8-bit LVDS synchronous busses.
SoC	System on a Chip.
SPB	Sundance Platform Bus. 50-way connector with multiple LVDS signals.
SSB	Sundance SRIO Bus.
USB	Universal Serial Bus.
VGA	Video Graphics Array. Used here to refer to the analog portion of the video signal.

3 Block Diagram



4 Circuit Description

The main component of the SMT-FMC211 is the Texas Instruments 4 channel DAC – DAC3484.

This device offers excellent SFDR performance better than 70dBc, with an output sample rate of over 312MSPS.

It interfaces to an FPGA using a 16 bit differential DDR bus.

The FPGA connects to two 16-bit wide DDR3 memory devices which act as a waveform store. Finally the FPGA also interfaces to a LPC (low pin count) FMC socket using the full 68 I/O pins available.

Configuration of the FPGA's internal registers is via a 2-pin I²C style bus.

The DAC outputs are buffered using 50 Ohm capable drivers with high SFDR. The DAC's clock is supplied externally as are two triggers for the FPGA.

The power supplies from the FMC connector are further regulated and filtered. Optionally, the board may be supplied from an external power input header.

4.1.1 FPGA

The FPGA is a Xilinx Artix-7 device in a CSG324 package.

Its internal fabric is configured at power on from a serial ROM device.

4.1.2 DAC

Set to operate at up to 312.5MSPS the DAC3484 provides a 16-bit sample word over a 16-bit differential bus.

The compliance voltage of the DAC should not exceed 0.5V to maintain performance.

4.1.3 FMC

A low pin count (LPC) interface is implemented on this module.

A 16 bit differential data interface connects the FMC to the FPGA. Two clocks are also provided.

An I²C bus also connects the FMC to the FPGA. This allows FPGA firmware registers to be accessed via the FMC carrier.

The +12V and +3.3V power rails are required. Data signalling levels are set using the Vadj FMC pins. Signal levels between 1.8V and 3.3V are acceptable.

4.1.4 Sample Clock

Separate inputs are provided for the DAC sample clock, SYNC signal. And FPGA clock. The use of a SYNC input allows ALL DAC outputs across multiple modules to be phase-aligned.

These clocks are typically driven from the clock generator/distributor of an SMT166 SLB/FMC carrier board. Alternatively, an on-board programmable PLL can produce the required timing signals.

The PLL is a CDCE620005 coupled with a CDCP1803 divider. The PLL device connects to the FPGA using a SPI interface.

4.1.5 Outputs and Buffers

Single ended DC-coupled analog outputs are provided on a Samtec 40-way connector. This is vertically mounted but a right angle adapter is available for use with an FMC bezel. A connector assembly converts this high-density connector into individual co-ax sockets.

The LTC6252 is a low noise buffer capable of driving 50 Ohm systems. It is a wide bandwidth unity gain stable op-amp capable of driving a 50 Ohm load. When presented with differential inputs each with a 0 to 500mV range, the output will be 1Vp-p (500mV peak), dependent upon feedback resistor values.

Recommended by Linear Technology for their high speed DACs.

These devices are powered by +/-2.5V from linear regulators, then through ferrite beads. The +2.5V linear regulator is supplied by the FMC 3.3V, whereas the -2.5V device requires a DCDC convertor to produce a negative rail.

4.1.6 Triggers

Three general purpose signals are available on the Samtec connector. These signals are amplitude limited to LVCMOS33 levels and otherwise DC-coupled directly to the FPGA.

4.1.7 Local Power Supplies

Custom designed DC-DC convertors provide a local supply which is then linear regulated and filtered for the ADC and output buffers.

4.1.8 Configuration

The FPGA is typically configured from on-board serial memory. It may also be configured via the JTAG signals present on the FMC connector.

4.1.9 Memory DDR3

Two 16-bit wide DDR3 memory devices are used on the FMC module to provide storage. This memory is directly accessible by the FPGA and its primary use is the storage of waveforms. A total of 256Mbytes is provided.

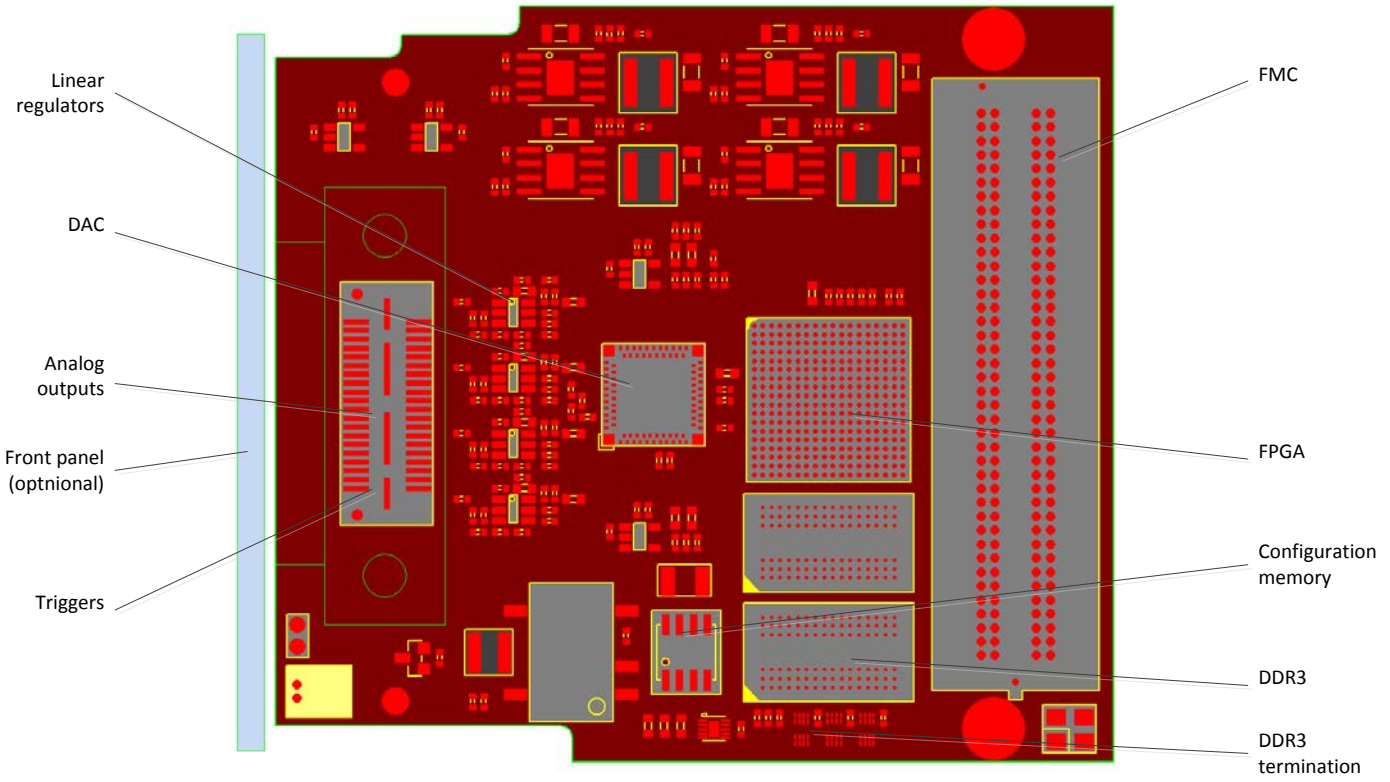
4.1.10 SPI Flash

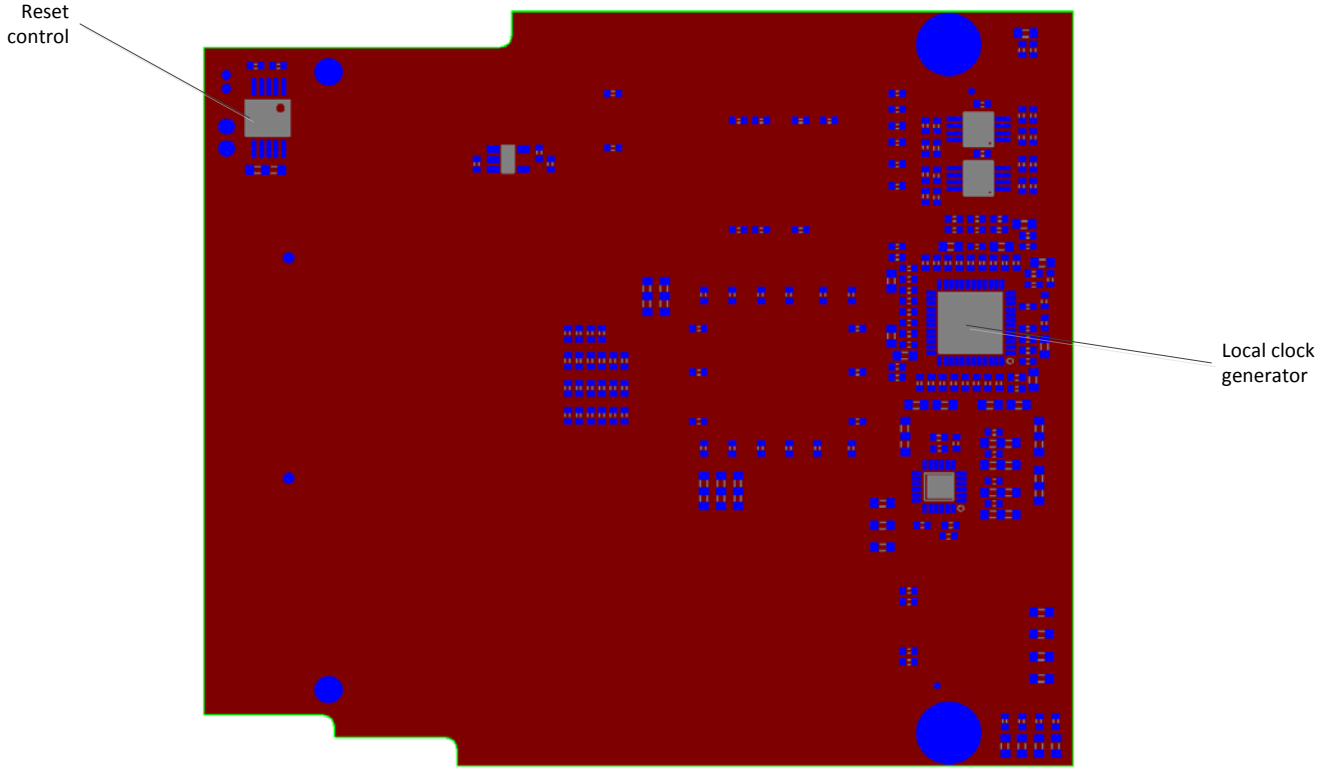
This 32Mbit serially accessible device holds the configuration for the FPGA.

4.1.11 LEDs

Three user LEDs are provided directly on the module primarily for debug use.

5 PCB Layout (top and bottom views)





6 Physical Properties

Dimension	82mm	69mm

Weight	

Voltage	Power (estimate)
+12V	
+3.3V	
Vadj	

RH	10-80%
Temperature	-10 to +40ºC -25 to +80ºC

MTBF	> 50,000 hours

PCB	8 layers 1.6mm thick 50 Ohm analog impedance

7 FMC Pin-Out (provisional)

FMC pin	Signal	FPGA pin	FMC pin	Signal	FPGA pin
C10	FMC_LA6_P		D8	FMC_LA1_P	
C11	FMC_LA6_N		D9	FMC_LA1_N	
C14	FMC_LA10_P		D11	FMC_LA5_P	
C15	FMC_LA10_N		D12	FMC_LA5_N	
C18	FMC_LA14_P		D14	FMC_LA9_P	
C19	FMC_LA14_N		D15	FMC_LA9_N	
C22	FMC_LA18_P		D17	FMC_LA13_P	
C23	FMC_LA18_N		D18	FMC_LA13_N	
C26	FMC_LA27_P		D20	FMC_LA17_P	
C27	FMC_LA27_N		D21	FMC_LA17_N	
C30	FMC_SCL		D23	FMC_LA23_P	
C31	FMC_SDA		D24	FMC_LS23_N	
			D26	FMC_LA26_P	
			D27	FMC_LA26_N	
			D29	FMC_TDI	-
			D30	FMC_TDO	-
			D31	FMC_TMS	-
			D33	FMC_TCK	-

G2	FMC_CLK1_P		H1	FMC_VREF	
G3	FMC_CLK1_N		H2	FMC_PRSNT	
G6	FMC_LA0_P		H4	FMC_CLK0_P	
G7	FMC_LA0_N		H5	FMC_CLK0_N	
G9	FMC_LA3_P		H7	FMC_LA2_P	
G10	FMC_LA3_N		H8	FMC_LS2_N	
G12	FMC_LA8_P		H13	FMC_LA7_P	
G13	FMC_LA8_N		H14	FMC_LA7_N	
G15	FMC_LA12_P		H16	FMC_LA11_P	
G16	FMC_LA12_N		H17	FMC_LA11_N	
G18	FMC_LA16_P		H19	FMC_LA15_P	
G19	FMC_LA16_N		H20	FMC_LA15_N	
G21	FMC_LA20_P		H22	FMC_LA19_P	
G22	FMC_LA20_N		H23	FMC_LA19_N	
G24	FMC_LA22_P		H25	FMC_LA21_P	
G25	FMC_LA22_N		H26	FMC_LA21_N	
G27	FMC_LA25_P		H28	FMC_LA24_P	
G28	FMC_LA25_N		H29	FMC_LA24_N	
G30	FMC_LA29_P		H31	FMC_LA28_P	
G31	FMC_LA29_N		H32	FMC_LA28_N	
G33	FMC_LA31_P		H34	FMC_LA30_P	
G34	FMC_LA31_N		H35	FMC_LA30_N	
G36	FMC_LA33_P		H37	FMC_LA32_P	
G37	FMC_LA33_N		H38	FMC_LA32_N	
G39	FMC_VADJ		H40	FMC_VADJ	

8 Verification, Review & Validation Procedures

To be carried out in accordance with the Sundance Quality Procedures (ISO9001).

9 Safety

This module presents no hazard to the user when in normal use.

10 EMC

This module is designed to operate from within an enclosed host system, which is built to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate enclosure.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.

11 Ordering Information

Order number:

SMT-FMC211-y

y:

C = Commercial temperature

I = Industrial temperature