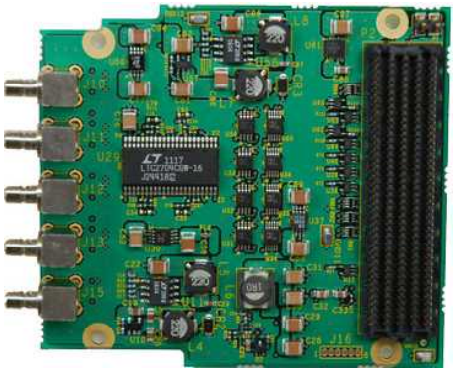
RFM-DACNF04-S250KH
(FMC DA board)
Hardware Reference Manual
Ver.1.0



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Revision History

Version	Date	Change Made
ver1.0	2013/05/23	First Release

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1) Preface

Thank you for choosing **RFM-DACNF04-S250KH** FMC board.
This manual describes the features and specifications of the **RFM-DACNF04-S250KH** FMC board.
Read and understand the contents of this manual before operating this board.

K.K.Rocky reserves the right to revise this document and to make changes without notice.

2) Safety Instructions

Always read the safety instructions carefully.

Cautions

- **If smoke or an abnormal odor is detected from the FMC board, power off and stop using the FMC board.**
  Continuous use of FMC board under these conditions might cause fire or permanent damage to the system. Contact K.K.Rocky to test and repair.

- **Do not attempt to disassemble and modify this board.**
  Disassembly and modification could cause fire or electric shock.
  Please contact K.K.Rocky for any repair and test service.

- **Never allow any liquids to spill on the FMC board, and never expose FMC board to water or moisture**.
  Exposure to liquid or moisture could cause electric shock or fire.

- **Avoid excessive vibration and any impact or shock to the FMC board.**
  Neglect could result in any damage on the board.

- **Avoid handling the FMC board while it is powered. Only handle by the edges to minimize the risk of electrostatic discharge damage.**

- **if the FMC board has been dropped and damaged, stop using the board and contact K.K.Rocky to repair.**

- **Never place the board where it will be exposed to excess heat, such as in direct sunlight, or near heater.**

1. Introduction

The RFM-DACNF04-S250KH is an ANSI/VITA57-1 compliant FPGA Mezzanine Card (FMC) which offers multi-purpose 4-channel DA converter up to 250KSPS.
It Works on a High Pin Count (HPC) site of FMC carrier board from K.K.Rocky or third party.

2. Main components

The main components of the board are listed on Table 2-1.

Table 2-1 Main Components

Item	Description	Remarks
FMC connector (HPC)	ASP-134488-01 (SAMTEC)	
DA converter	LTC2704-16 (Linear Technology)	
Offset adjuster	AD5623RBRMZ-5 (ADI)	
Offset output AMP	AD822ARMZ (ADI)	
EEPROM (I2C)	BR24L01AFV-WE2 (Rohm)	
Front side Coaxial connector	414026-3 (Tyco)	

3. Block Diagram

Figure 3-1 shows the block diagram of the board.

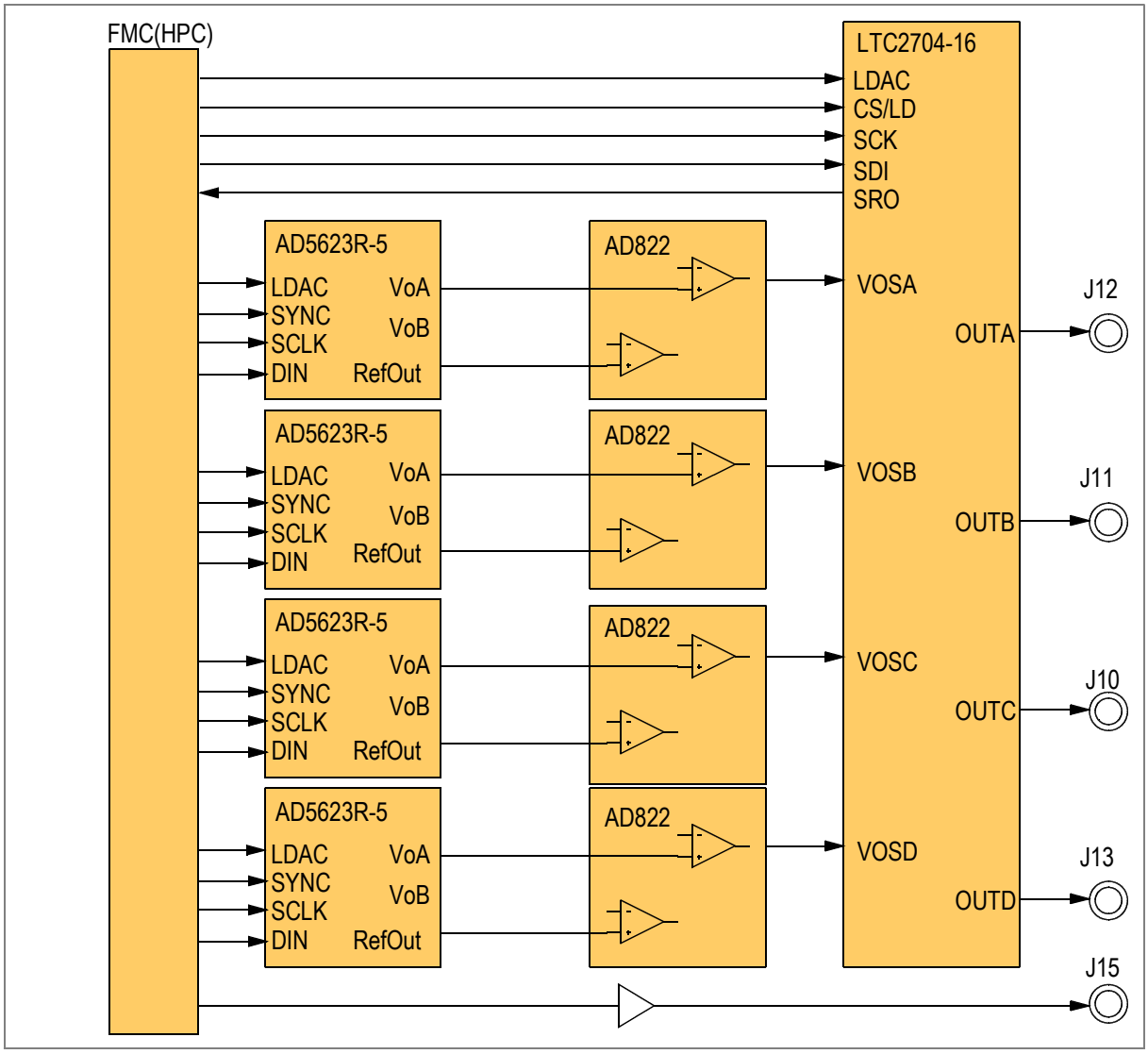

Figure 3-1 Block Diagram

An offset of each Chanel on LTC2704-16 can be applied individually through AD5623RBRMZ-5 and AMP-AD822ARMZ. You can control AD5623RBRMZ-5 through SPI from FMC carrier board.

DAC data should be set through SPI on LTC2704-16.

Please refer data sheet provided by Linear Technology and Analog devices, for detail of SPI timing and commands.

4. Board Layout

Figure 4-1 shows the board layout of RFM-DACNF04-S250KH.

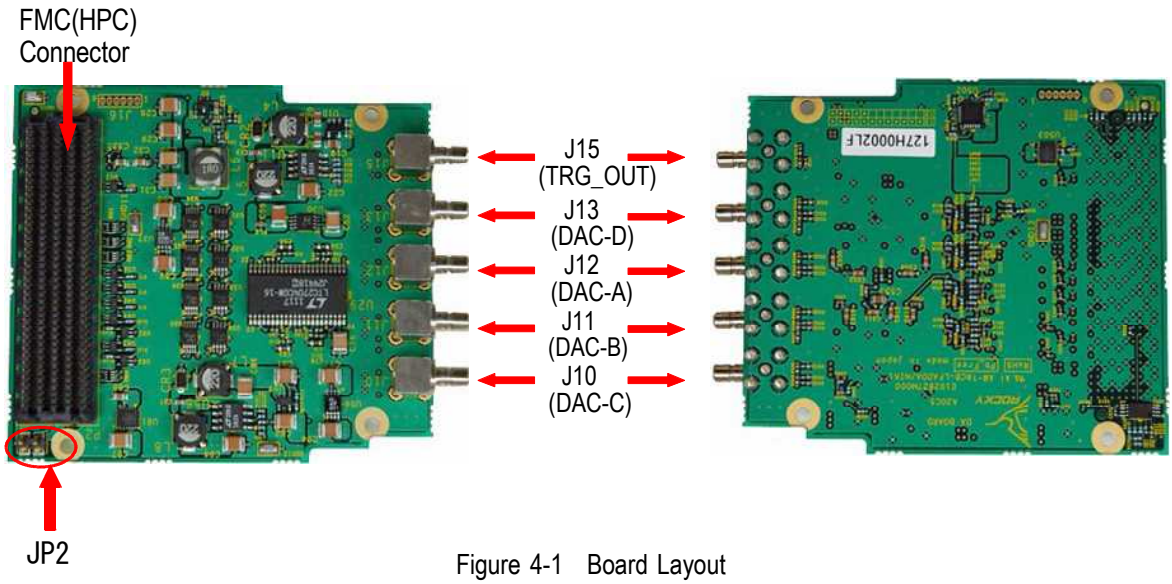

Figure 4-1 Board Layout

Table 4-1 Description of connectors

Item	Description	Remarks
FMC connector	FMC connector (High-Pin Count)	ASP-134488-01 (SAMTEC)
J10～J13	D/A analogue output	414026-3 (Tyco)
J15	Trigger output (LVCMOS_25)	414026-3 (Tyco)
JP2	EEPROM control	HWP-2P-G-M (MAC8)

5. Board Specifications

5.1 Output Signals

Table 5-1 shows the specification of DA output signals.

Table 5-1 specification of DA output signals

Item	Description
Number of channels	4 channels
Resolution	16 bits
DA bandwidth	DC to 250Khz
Coupling	DC coupling
Impedance	50-ohm (single ended)
Output level	Selectable one out of following four, with command setting to LTC2704-16.. 1) 0 to +5V, 2) -5 to +5V, 3) 0 to +10V, 4) -10 to +10V

5.2 Power

Table 5-2 shows input power for the board. All the power are supplied from FMC HPC connector.

Table 5-2 Power

Item	Voltage	Current	Remarks
12P0V	+12V	80 mA (Max)	
3P3V	+3.3V	0.5 mA (Max)	
VADJ	+2.5V	0A	VADJ is only looped back to VIO_M2C
3P3VAUX	+3.3V	3 mA (Max)	

Figure 5-1 shows the block diagram of power distribution.

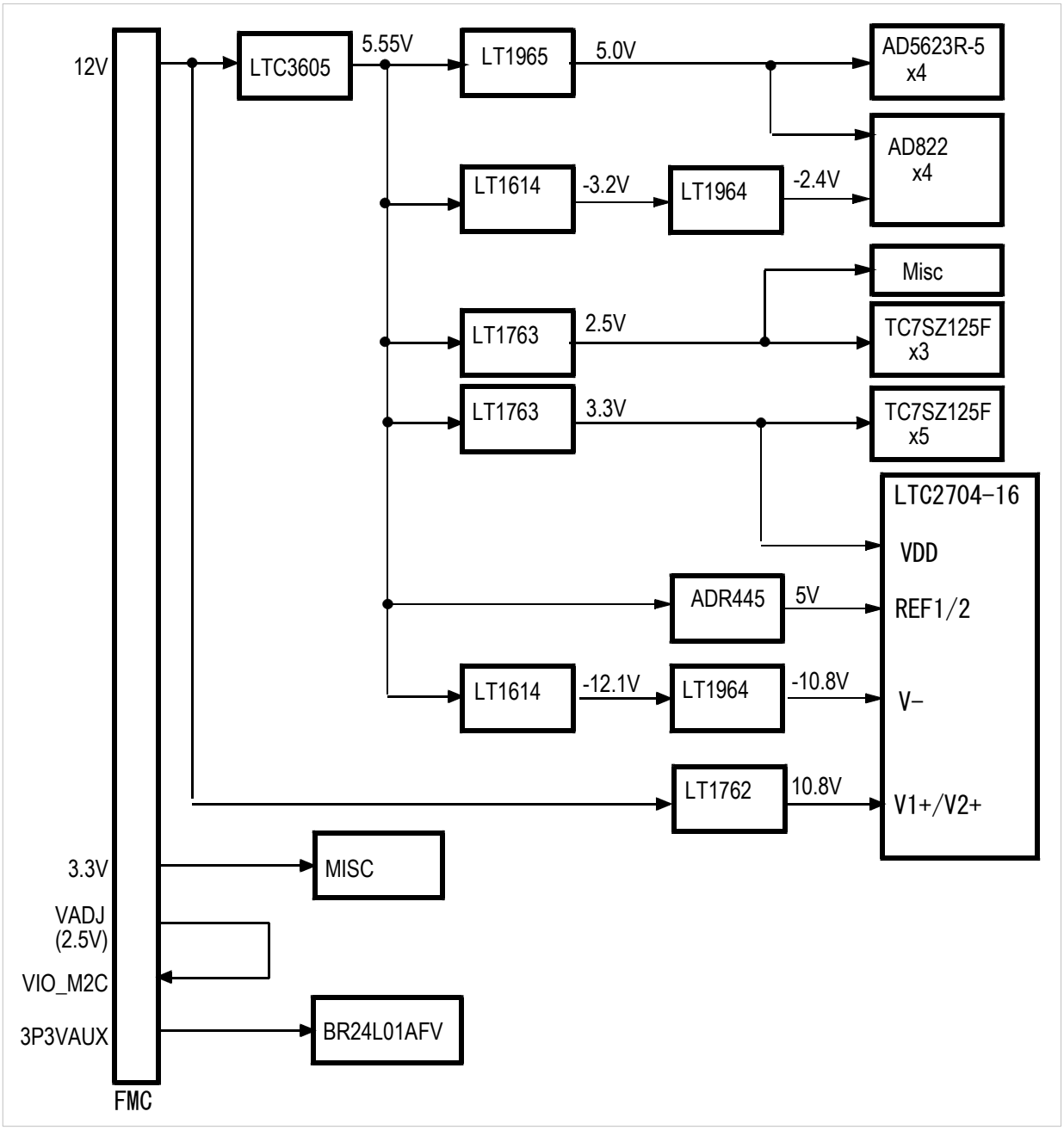

Figure 5-1 Power Distribution

5.3 Jumper

Table 5-2 shows the function of JP2.

Table 5-2 JP2 Function

JP2 Setting	Description
Off	Normal Operation, (Disable to write EEPROM)
On	Set jumper to enable writing EEPROM.

5.4 DAC Circuit

Figure 5-2 shows the outline of the circuit.

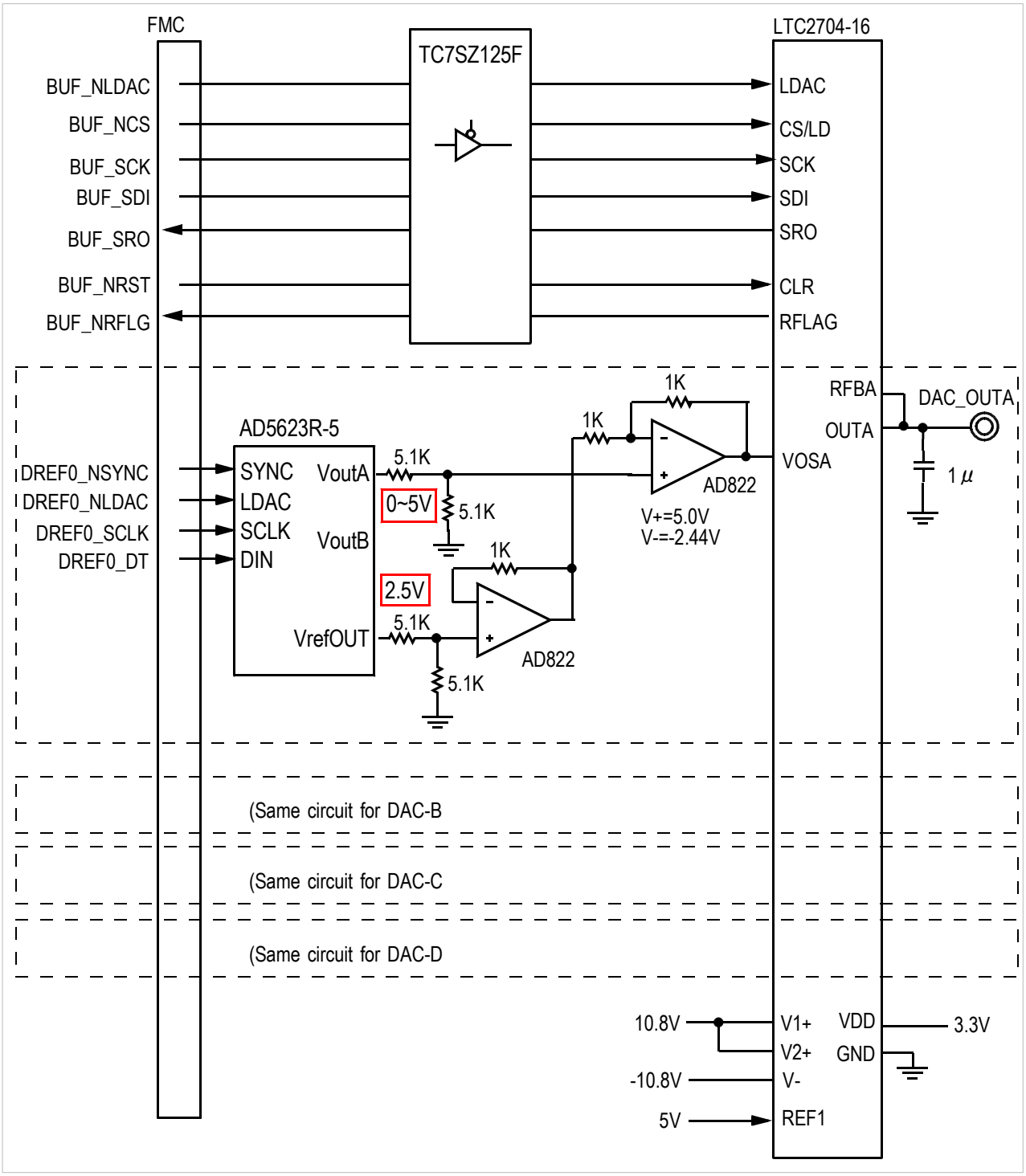

Figure 5-2 Circuit outline

5.5 FMC Connector Pin Assignment

Table 5-3 shows pin assignment of FMC connector.

Table 5.3 Connector Pin Assignment

	K	J	H	G	F	E	D	C	B	A
1	N.C.	GND	N.C.	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND
2	GND	N.C.	PRSNT_M2C_L	CLK1_M2C_P	GND	N.C.	GND	N.C.	GND	N.C.
3	GND	N.C.	GND	CLK1_M2C_N	GND	N.C.	GND	N.C.	GND	N.C.
4	N.C.	GND	N.C.	GND	N.C.	GND	N.C.	GND	N.C.	GND
5	N.C.	GND	N.C.	GND	HA00_N_CC	GND	N.C.	GND	N.C.	GND
6	GND	N.C.	GND	N.C.	GND	N.C.	GND	N.C.	GND	N.C.
7	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	GND	N.C.	GND	N.C.
8	N.C.	GND	N.C.	GND	N.C.	GND	N.C.	GND	N.C.	GND
9	GND	N.C.	GND	N.C.	GND	N.C.	N.C.	GND	N.C.	GND
10	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	GND	N.C.	GND	N.C.
11	N.C.	GND	N.C.	GND	N.C.	GND	N.C.	N.C.	GND	N.C.
12	GND	HA11_P	GND	N.C.	GND	N.C.	N.C.	GND	N.C.	GND
13	HA10_P	HA11_N	N.C.	N.C.	N.C.	N.C.	GND	GND	N.C.	GND
14	HA10_N	GND	N.C.	GND	N.C.	GND	N.C.	N.C.	GND	N.C.
15	GND	HA14_P	GND	N.C.	GND	N.C.	N.C.	N.C.	GND	N.C.
16	HA17_P_CC	HA14_N	N.C.	N.C.	N.C.	N.C.	GND	GND	N.C.	GND
17	HA17_N_CC	GND	N.C.	GND	N.C.	GND	N.C.	GND	N.C.	GND
18	GND	HA18_P	GND	N.C.	GND	N.C.	N.C.	N.C.	GND	N.C.
19	HA21_P	HA18_N	N.C.	N.C.	N.C.	N.C.	GND	N.C.	GND	N.C.
20	HA21_N	GND	N.C.	GND	N.C.	GND	N.C.	GND	N.C.	GND
21	GND	HA22_P	GND	N.C.	GND	N.C.	N.C.	GND	N.C.	GND
22	HA23_P	N.C.	N.C.	N.C.	N.C.	N.C.	GND	N.C.	GND	N.C.
23	N.C.	GND	N.C.	GND	N.C.	GND	N.C.	N.C.	GND	N.C.
24	GND	N.C.	GND	N.C.	GND	N.C.	N.C.	GND	N.C.	GND
25	HB00_P_CC	N.C.	N.C.	N.C.	N.C.	N.C.	GND	GND	N.C.	GND
26	N.C.	GND	N.C.	GND	N.C.	GND	N.C.	N.C.	GND	N.C.
27	GND	HB07_P	GND	N.C.	GND	N.C.	N.C.	N.C.	GND	N.C.
28	HB06_P_CC	N.C.	N.C.	N.C.	N.C.	N.C.	GND	GND	N.C.	GND
29	N.C.	GND	N.C.	GND	N.C.	GND	N.C.	GND	N.C.	GND
30	GND	N.C.	GND	N.C.	GND	N.C.	TDI	SCL	GND	N.C.
31	HB10_P	N.C.	N.C.	N.C.	N.C.	N.C.	TDO	SDA	GND	N.C.
32	N.C.	GND	N.C.	GND	N.C.	GND	3P3VAUX	GND	N.C.	GND
33	GND	N.C.	GND	N.C.	GND	N.C.	N.C.	GND	N.C.	GND
34	HB14_P	N.C.	N.C.	N.C.	N.C.	N.C.	N.C.	GA0	GND	N.C.
35	N.C.	GND	N.C.	GND	N.C.	GND	GA1	12P0V	GND	N.C.
36	GND	HB18_P	GND	N.C.	GND	N.C.	3P3V	GND	N.C.	GND
37	HB17_P_CC	HB18_N	N.C.	N.C.	N.C.	N.C.	GND	12P0V	N.C.	GND
38	HB17_N_CC	GND	N.C.	GND	N.C.	GND	3P3V	GND	GND	N.C.
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	N.C.
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	N.C.	GND
	HPC		LPC		HPC		LPC		HPC	

Note: N.C. means #No Connection"

(1) Supply +2.5V to VADJ.
(2) FMC loops back VADJ to VIO_B_M2C.

Table 5-4 shows the FMC pin assignment of the board.

Table 5-4 The Signal Assignment to FMC connector

Pin#		Signal Name	FMC_LOC	I/O	Description	Remarks	
LTC2704-16 SPI signal							
K	25	BUF_SCK	HB00_P_CC	I	DAC SPI clock	LT2704-16	SCK
K	28	BUF_SDO	HB06_P_CC	O	DAC SPI data output		SRO
J	27	BUF_NCS	HB07_P	I	DAC SPI chip select		CS/LD
K	31	BUF_NLDAC	HB10_P	I	DAC LDAC_n input		LDAC
K	34	BUF_NRFLG	HB14_P	O	DAC reset flag output		RFLAG
J	21	BUF_NRST	HA22_P	I	DAC reset		CLR
K	22	BUF_SDI	HA23_P	I	DAC SPI data input		SDI
AD5623R-5 SPI Signal (offset to DAC-A)							
K	13	DREF0_NSYNC	HA10_P	I	Offset0 AD5623R SYNC input	AD5623R-5	SYNC
K	14	DREF0_DT	HA10_N	I	Offset0 AD5623R SPI data input		DIN
J	12	DREF0_NLDAC	HA11_P	I	Offset0 AD5623R LDAC input		LDAC
J	13	DREF0_SCLK	HA11_N	I	Offset0 AD5623R SPI clock input		SCLK
AD5623R-5 SPI signal (offset to DAC-B)							
K	37	DREF1_NSYNC	HB17_P_CC	I	Offset1 AD5623R SYNC input	AD5623R-5	SYNC
K	38	DREF1_DT	HB17_N_CC	I	Offset1 AD5623R SPI data input		DIN
J	36	DREF1_NLDAC	HB18_P	I	Offset1 AD5623R LDAC input		LDAC
J	37	DREF1_SCLK	HB18_N	I	Offset1 AD5623R SPI clock input		SCLK
AD5623R-5 SPI signal (offset to DAC-C)							
K	19	DREF2_NSYNC	HA21_P	I	Offset2 AD5623R SYNC input	AD5623R-5	SYNC
K	20	DREF2_DT	HA21_N	I	Offset2 AD5623R SPI data input		DIN
J	18	DREF2_NLDAC	HA18_P	I	Offset2 AD5623R LDAC input		LDAC
J	19	DREF2_SCLK	HA18_N	I	Offset2 AD5623R SPI clock input		SCLK
AD5623R-5 SPI signal (offset to DAC-D)							
K	16	DREF3_NSYNC	HA17_P_CC	I	Offset3 AD5623R SYNC input	AD5623-R	SYNC
K	17	DREF3_DT	HA17_N_CC	I	Offset3 AD5623R SPI data input		DIN
J	15	DREF3_NLDAC	HA14_P	I	Offset3 AD5623R LDAC input		LDAC
J	16	DREF3_SCLK	HA14_N	I	Offset3 AD5623R SPI clock input		SCLK
F	5	DTRG_OUT	HA00_N_CC	I	DA trigger output		
Other signals							
B	1	CLK_DIR	CLK_DIR	O	Clock direction		
C	30	SCL	SCL	I	FMC I2C clock input		
C	31	SDA	SDA	I/O	FMCI2C address/data		
C	34	GA0	GA0	I	FMCI2C address 0	Pulled up to 3P3VAUX	
D	35	GA1	GA1	I	FMCI2C address 1	Pulled up to 3P3VAUX	
D	30	TDI	TDI	I	JTAG data input	looped back to TDO	
D	31	TDO	TDO	O	JTAG data output		
F	1	PG_M2C	PG_M2C	O	Module power good		
G	2	CLK1_M2C_P	CLK1_M2C_P	O		Pulled up to VADJ	
G	3	CLK1_M2C_N	CLK1_M2C_N	O		Pulled down to GND	
H	2	PRSNT_M2C_L	PRSNT_M2C_L	O	Module present signal	Pulled down to GND	

6. Operation

(1) Set AD5623R-5 to use internal reference. (With this setting REFOUT outputs 2.5V)
(2) Set Offset Voltage with setting AD5623R-5 when it is necessary.
AD5623R-5 generate 0 to 5V, which generate VOSx -1.25V to 3.75V.
(3) Set LTC2704 to what you want.

Refer to the LTC2704 (Linear Technology) data sheet and AD5623R (Analog Devices) data sheet for detail.